SYSTEM

User Guide

PC3-ALLEGRO • *CompactPCI*® PlusIO CPU Card

Intel® Core™ i7-3xxx Processor Quad-Core (Ivy Bridge)

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Contents

About this Manual

This manual describes the technical aspects of the PC3-ALLEGRO, required for installation and system integration. It is intended for the experienced user only.

Edition History

Ed.	Contents/*Changes*	Author	Date
1	User Manual PC3-ALLEGRO, english, preliminary edition Text #7106, File: pc3_ug.wpd	mib	2013-09-09
2	Error corrected on pg.44 , upper and lower table	mib	2013-09-25
3	Reworked section “Watchdog”	gn	2013-12-06
4	Power Requirements updated	mib	2013-12-11
5	Reworked sections Serial ATA Interface and High Speed Expansion Connector J-HSE	mib	2014-01-10
6	Modified block diagram - RIO SATA configured to 3G by default	jj	15 January 2014
7	Table Feature Summary updated	jj	17 February 2014
8	Table Power Requirements updated	mib	3 April 2014
9	Table CompactPCI J2 updated	mib	20 June 2014
10	Added list of local pci devices, SDVO option removed on J-SDVO	mib	21 July 2014
11	Added photos PC3 w. PCL Side Card Assembly	jj	31 July 2014
12	Added photo PC3 w. PCL Side Card Assembly Exploded View	jj	11 August 2014
13	Added ‘Board Control and Status Registers’, updated links	mib	21 August 2014
14	Added note on operation in systems with a 64-bit CompactPCI® backplane	mib	4 September 2014
15	Added additional function of HD LED	mib	18 September 2014
16	Added Power Requirements	mib	12 December 2014
17	Clarified resetting of UEFI BIOS settings to factory defaults	gn	16 January 2015
18	Universal V(I/O) on CPCI Interface	mib	27 January 2015
19	Added power requirements	mib	5 February 2015
20	Updated description of BCSR Status Registers 0 and 1, cleanup section “Watchdog”	gn	7 April 2015
21	Added photos PC3-ALLEGRO with C47-MSATA & C48-M2	jj	27 May 2015
22	Updated LM87 Information	mib	28 May 2015
23	Table 'Feature Summary' BIOS replaced by Firmware (UEFI) Table 'Reference Documents' UEFI & ACPI specifications	jj	14 August 2015
24	Removed redundant Operating Conditions	mib	3 September 2015
25	4HP Front panel illustration fixed marking for backplane Ethernet LED = EB, added 8HP and 12HP front panel illustrations	jj	23 September 2015
26	Table 'Feature Summary', added RT OS support	jj	30 September 2015
27	Completed Information about SATA on J-HSE	mib	22 January 2016

Ed.	Contents/*Changes*	Author	Date
28	Fixed typo in block diagram regarding J2 PCIe resources	jj	29 November 2016
29	Screw locking options for mDP connectors	jj	13 December 2016
30	Added Celeron® CPU to table 'Feature Summary'	jj	6 April 2017
31	Added photo USB cable connector fixation	jj	19 June 2017
32	Changed EMC regulation EN55022 --> EN55032 (Emission Requirements)	jj	25 November 2019

Related Documents

Related Information PC3-ALLEGRO	
PC3-ALLEGRO Home	www.ekf.com/p/pc3/pc3.html
PC3-ALLEGRO Product Information	www.ekf.com/p/pc3/pc3_pi.pdf

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- Chief River, Ivy Bridge, Panther Point, Core i7: ® Intel
- CompactPCI, CompactPCI PlusIO, CompactPCI Serial: ® PICMG
- Windows XP, Windows 7: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Reference Documents		
Term	**Document**	**Origin**
CFast™	CFast™ Specification Rev. 1.0	www.compactflash.org
CompactPCI®	CompactPCI Specification, PICMG® 2.0 R3.0, Oct. 1, 1999	www.picmg.org
CompactPCI® PlusIO	CompactPCI PlusIO Specification, PICMG® 2.30 R1.0, November 11, 2009	www.picmg.org
CompactPCI® Serial	CompactPCI Serial Specification, PICMG® CPCI-S.0 R1.0, March 2, 2011	www.picmg.org
DisplayPort	VESA DisplayPort Standard Version 1.1a January 11, 2008 VESA Mini DisplayPort Connector Standard Version 1 October 26, 2009	www.vesa.org
DVI	Digital Visual Interface Rev. 1.0 Digital Display Working Group	www.ddwg.org
Ethernet	IEEE Std 802.3, 2000 Edition	standards.ieee.org
LPC	Low Pin Count Interface Specification, Revision 1.1	developer.intel.com/design/chipsets/industry/lpc.htm
HD Audio	High Definition Audio Specification Rev.1.0	www.intel.com/design/chipsets/hdaudio.htm
PCI Express®	PCI Express® Base Specification 3.0	www.pcisig.com
SATA	Serial ATA 2.5/2.6 Specification Serial ATA 3.0 & 3.1 Specification	www.sata-io.org
UEFI	Unified Extensible Firmware Interface UEFI Specification Version 2.5 ACPI Specification Version 6.0	www.uefi.org
USB	Universal Serial Bus 3.0 Specification, Revision 1.0 November 12, 2008	www.usb.org

Overview

The PC3-ALLEGRO is a rich featured high performance 4HP/3U CompactPCI® PlusIO CPU board, equipped with a 3rd Generation Intel® Core™ i7 Ivy Bridge + ECC (dual- or quad-core) mobile processor based on 22nm technology. The PC3-ALLEGRO front panel is provided with two Gigabit Ethernet jacks, two USB 3.0 receptacles, and two Mini-DisplayPort connectors for attachment of high resolution digital displays, configured e.g. as extended desktop (option VGA).

The PC3-ALLEGRO is equipped with up to 16GB RAM with ECC support. 8GB memory-down are provided for rugged applications, and another 8GB are available via the DDR3 ECC SO-DIMM socket. The PC3-ALLEGRO backplane connectors comply with the PICMG® CompactPCI® PlusIO system slot specification, suitable for a rear I/O module or hybrid CompactPCI® Serial Systems. Several low profile mezzanine modules are available as mass storage solution.

CompactPCI® PlusIO (PICMG 2.30) is a new standard for rear I/O across J2, specified by the PICMG®. High speed signal lines (PCI Express®, SATA, Gigabit Ethernet and USB) are passed from the PC3-ALLEGRO through the special UHM connector to the backplane, for usage either on a PlusIO rear I/O transition module, or CompactPCI® Serial card slots.

CompactPCI® Serial (PICMG CPCIS.0) defines a completely new card slot, based on PCI Express®, SATA, Gigabit Ethernet and USB serial data lines. On a hybrid backplane, both card styles can reside, CompactPCI® and CompactPCI® Serial, with the PC3-ALLEGRO in the middle as system slot controller for both backplane segments.

The PC3-ALLEGRO is equipped with a set of local expansion interface connectors, which can be optionally used to attach a mezzanine side board. A variety of expansion cards is available, e.g. providing legacy I/O and additional PCI Express® based I/O controllers such as SATA, USB 3.0 and Gigabit Ethernet, or a third video output. Most mezzanine side cards can accommodate in addition a 2.5-inch drive.

Typically, the PC3-ALLEGRO and the related side card would come as a readily assembled 8HP unit. As an alternate, low profile Flash based mezzanine storage modules are available that fit on the PC3-ALLEGRO while maintaining the 4HP profile. The C48-M2 module e.g. is equipped with two M.2 SATA Solid State Drives (SSD), suitable for installation of any popular operating system.


USB
PG
GP
DP
DP
ETH
1
RB
HD
EB
2

Technical Features

Feature Summary

Feature Summary
▸ **CompactPCI® PlusIO (PICMG® CPCI 2.30) System Slot Controller**
▸ J1 Connector for Full CompactPCI® Classic 32-Bit Support, universal V(I/O) (3.3V or 5V)
▸ J2 Connector (UHM High Speed) for CompactPCI® PlusIO Support
▸ 4 x PCIe
▸ 4 x SATA
▸ 4 x USB
▸ 2 x GbE
▸ **Proven Intel® Mobile CPU Technology**
▸ 3rd Generation Intel® Core™ Mobile + ECC CPU, Code Name Ivy Bridge
▸ i7-3612QE Processor 2.1GHz • 35W TDP Standard Voltage Quad-Core
▸ i7-3555LE Processor 2.5GHz • 25W TDP Low Voltage Dual-Core
▸ i7-3517UE Processor 1.7GHz • 17W TDP Ultra Low Voltage Dual-Core
▸ *i5-3610ME Processor 2.7GHz • 35W TDP Standard Voltage Dual-Core*
▸ *i3-3120ME Processor 2.4GHz • 35W TDP Standard Voltage Dual-Core*
▸ *i3-3217UE Processor 1.6GHz • 17W TDP Ultra Low Voltage Dual-Core*
▸ Celeron® 1047UE Processor 1.4GHz • 17W TDP Ultra Low Voltage Dual-Core
▸ Intel® *QM77 Panther Point* Platform Controller Hub (PCH)
▸ **Integrated HD Graphics Engine, 3 Independent Displays, Enhanced Media Processing**
▸ Up to 3 Display Configuration (Front Panel: Dual mDP or Single VGA Connector Option)
▸ Max Resolution 2560 x 1600 (DisplayPort), 1920 x 1200 (VGA)
▸ 3rd Display via Side Card PCS-BALLET
▸ **Integrated Memory Controller up to 16GB DDR3 +ECC 1600**
▸ DDR3 +ECC Soldered Memory up to 8GB
▸ DDR3 +ECC SO-DIMM Memory Module Socket up to 8GB
▸ **SATA 6G &3G for Mass Storage**
▸ 2 + 2 SATA Channels 6Gbps/3Gbps for Mezzanine Storage Modules (Connector HSE)
▸ CompactFlash® Card with C40-SCFA Mezzanine Module Option (4HP Maintained)
▸ CFast™ Card with C41-CFAST Mezzanine Module Option (4HP Profile Maintained)
▸ SATA 1.8-Inch Solid State Drive with C42-SATA Mezzanine Card Option (4HP Maintained)
▸ Dual mSATA Modules with C47-MSATA RAID Mezzanine Card Option (4HP Maintained)
▸ 4 x SATA RAID Channels to UHM Connector J2, for RIO Module or CPCI Serial Backplane Usage, limited to 3G SATA by CPCI PlusIO Specification
▸ Hardware RAID Enabled by Marvell 88SE9230 ARM Powered Subsystem
▸ RAID Configuration Level 0/1/10

Feature Summary

- **USB 3.0 XHCI SuperSpeed & USB 2.0 EHCI Support**
- 2 x USB 3.0 F/P Connectors
- 6 x USB 2.0 to Mezzanine Connectors
- 4 x USB 2.0 to J2 (Backplane)

- **Gigabit Ethernet Controllers**
- 2 x GbE F/P RJ-45 Jacks
- 2 x GbE to Backplane Connector J2

- **PCI Express® Based Design for Component Interconnect**
- PCI Express® for System Expansion by Mezzanine and Backplane or RIO
- 4 x PCI Express® Gen2 Lanes to CPCI PlusIO Backplane J2 Connector
- 4 x PCI Express® Gen2 Lanes to Mezzanine Connector

- **Set of Mezzanine Connectors for Storage Module or Side Card**
- Legacy I/O Mezzanine Expansion Connector EXP (USB, HD Audio, LPC)
- High Speed I/O Mezzanine Expansion Connector HSE (4 x SATA, 4 x USB)
- PCI Express® Mezzanine Expansion Connector PCIE (4 Lanes)
- Third Display Mezzanine Expansion Connector DP
- Variety of Mezzanine Expansion Boards (Side Cards) Available
- Most Mezzanines Optionally Equipped with 2.5-Inch Single- or Dual-Drive
- Low Profile Storage Modules Maintain 4HP F/P Width
- Side Cards with Additional Front Panel I/O Connectors (8HP & 12HP Assembly

- **Phoenix® UEFI** (Unified Extensible Firmware Interface) with CSM*
- Fully Customizable by EKF
- Secure Boot on Request
- Windows®, Linux and other (RT)OS' Supported

** CSM (Compatibility Support Module) emulates a legacy BIOS environment, which allows to boot a legacy operating system such as DOS, 32-bit Windows and some RTOS'*

- **Best Suited e.g. for Industrial, Transportation & Instrumentation Applications**
- Long Term Availability
- Rugged Solution
- Coating, Sealing, Underfilling Available on Request

Feature Summary

- **Regulation & Environmental**
- RoHS compliant
- EC Regulations EN55032, EN55024, EN60950-1 (UL60950-1/IEC60950-1)
- Operating Temperature: 0°C to +70°C (Industrial Temperature Range on Request)
- Storage Temperature: -40°C to +85°C, max. Gradient 5°C/min
- Humidity 5% ... 95% RH non Condensing
- Altitude -300m ... +3000m
- Shock 15g 0.33ms, 6g 6ms
- Vibration 1g 5-2000Hz
- MTBF 104 x 10^3 h (11.9 years) @ 50°C
- Designed & Manufactured in Germany
- ISO 9001 Certified Quality Management

- **RT OS Board Support Packages & Driver**
- LynxOS - on request
- On Time RTOS-32 - on request
- OS-9 - on request
- QNX 4.x, 6.x - on request
- Real-Time Linux (RT Patch) - on request
- RTX - on request
- VxWorks 6.9 - under development
- VxWorks 7.0 - on request
- Others - on request

Performance Rating

Performance Rating
tbd

Operating Conditions

Operating Conditions	
Thermal & Environmental Conditions	▸ Operating Temperature 0°C to +70°C (-40°C to +85°C on Request) ▸ Storage temperature: -40°C to +85°C, max. Gradient 5°C/min ▸ Humidity 5% ... 95% RH non Condensing ▸ Altitude -300m ... +3000m ▸ Shock 15g 0.33ms, 6g 6ms ▸ Vibration 1g 5-2000Hz
EC Regulations	▸ EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1) ▸ 2002/95/EC (RoHS)
MTBF	104 x 10^3 h (11.9 years) @ 50° C

Power Requirements

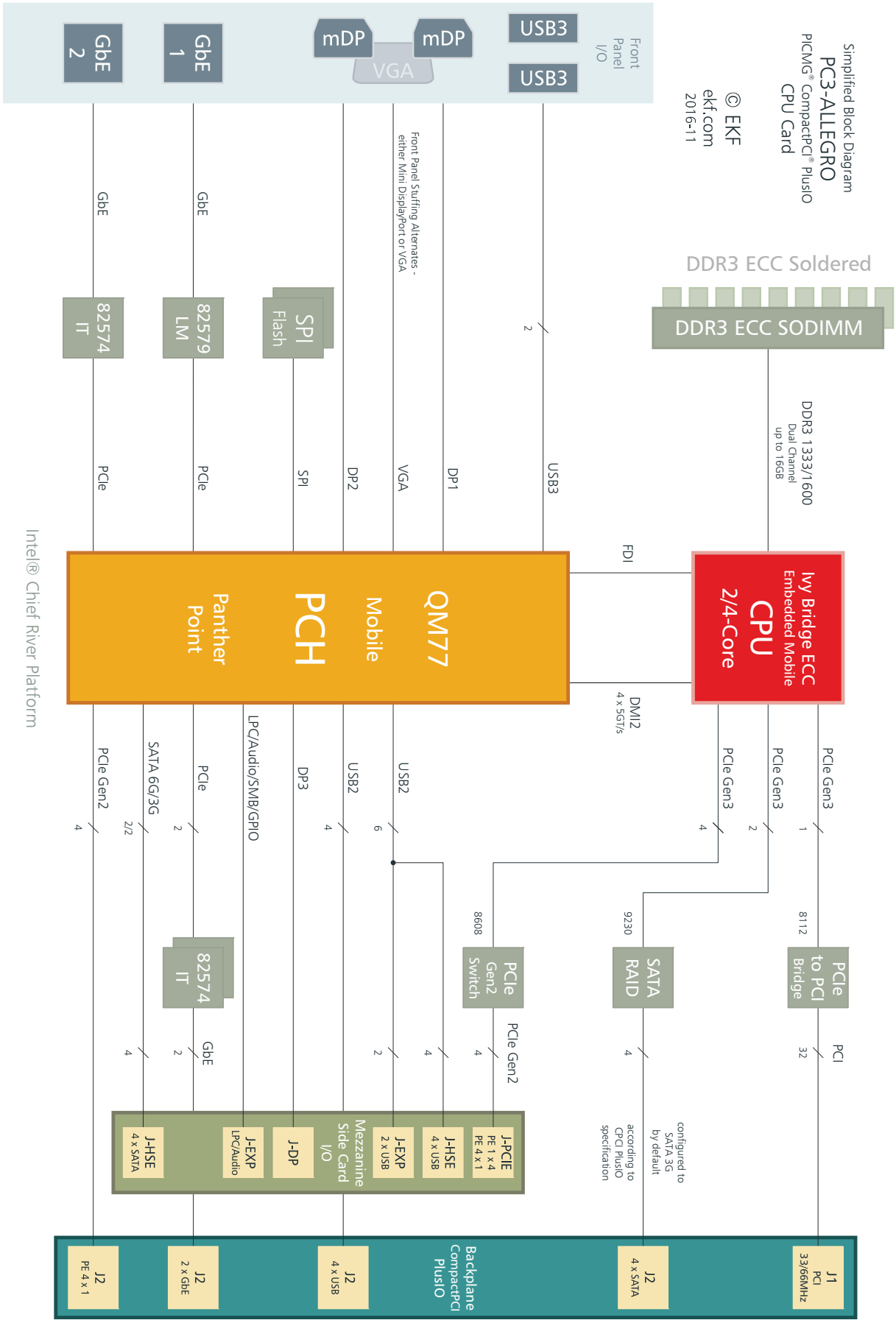
Power Requirements				
	Load Current [A] at +3.3V (+0.17V/-0.1V)		Load Current [A] at +5V (+0.25V/-0.15V)	
Board	Maximum Performance LFM / HFM / Turbo [1]	Windows 7 Idle LFM / HFM / Turbo [1]	Maximum Performance LFM / HFM / Turbo [1]	Windows 7 Idle LFM / HFM / Turbo [1]
PC3-68XX	5.0 / 5.0 / 5.0 [2]	2.7 / 2.7 / 2.7 [2]	6.9 / 7.1 / 8.7	0.8 / 0.8 / 0.8
PC3-48XX	4.1 / 4.1 / 4.1 [2]	2.7 / 2.7 / 2.7 [2]	4.3 / 5.1 / 5.5	0.8 / 0.8 / 0.8
PC3-22XX	TBD / TBD / TBD [2]	TBD / TBD / TBD [2]	TBD / TBD / TBD	TBD / TBD / TBD
PC3-046X [3]	- / 2.65 / - [2]	1.9 / 1.9 / - [2]	- / 2.45 / -	0.7 / 0.7 / -

[1] Intel SpeedStep Frequence Modes LFM: Low Frequency Mode, HFM: High Frequency Mode.

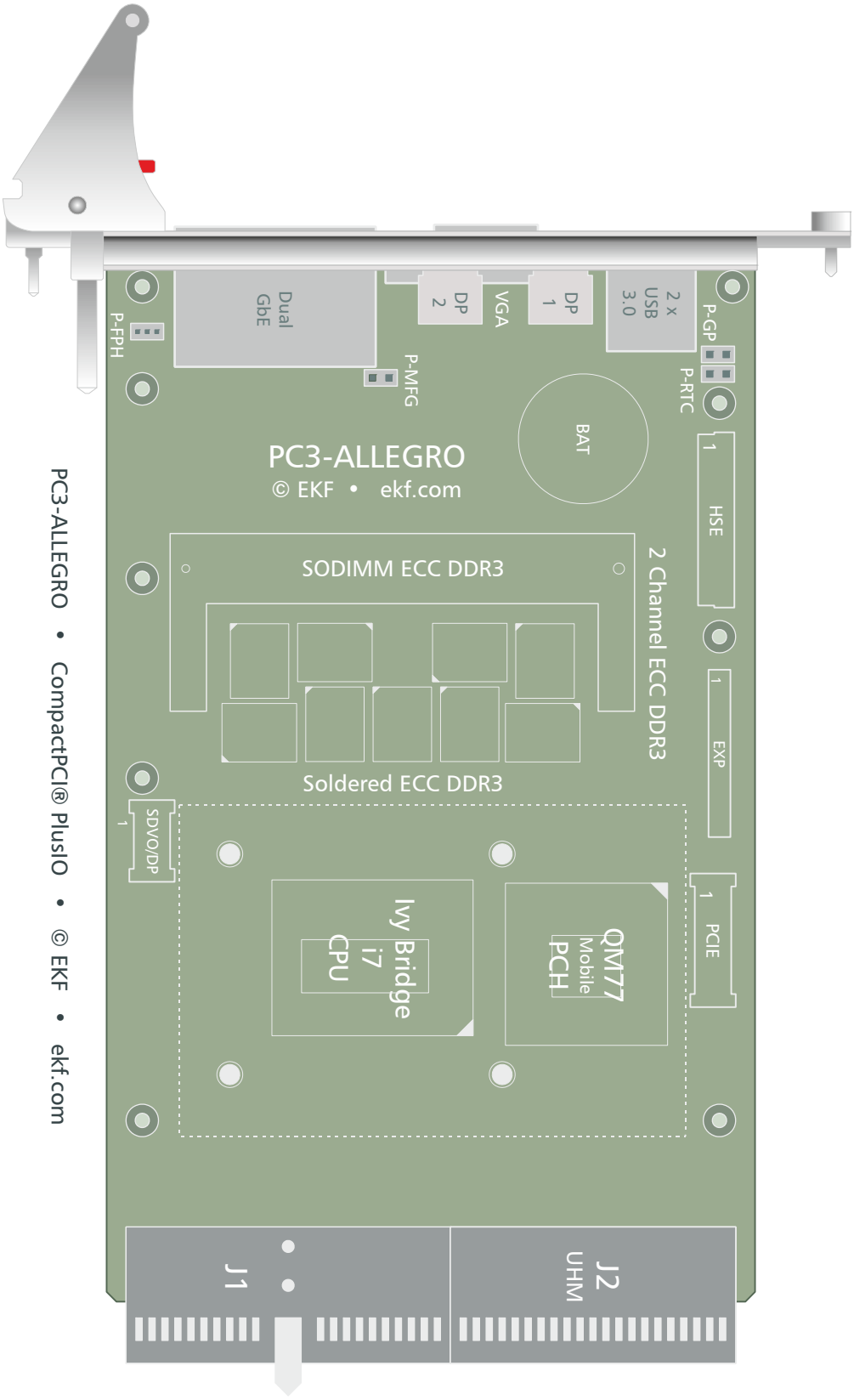
[2] Add 200/600mA (link only/active) @1Gbps per Ethernet Port.

[3] For Intel Celeron-1047UE there is no Turbo Mode at all and no low Frequency Mode at workload.

Block Diagram



Top View Component Assembly



Front Panel Connectors

ETH1/2	Dual Gigabit Ethernet RJ-45 receptacles with integrated indicator LEDs
mDP1/2	Mini DisplayPort digital video output receptacle (VGA connector available as alternate)
USB1/2	Universal Serial Bus 3.0 type A receptacles
VGA	VGA analog video output connector (Mini DisplayPort connectors available as alternate)

Front Panel Switches & Indicators

EB	LED indicating Backplane Ethernet activity
FPH	Front Panel Handle with integrated switch (programmable function, power event button by default)
GP	General Purpose bicolour LED
HD	LED indicating any activity on SATA ports
PG	Power Good/Board Healthy bicolour LED
RST	System Reset Button (Option)

On-Board Connectors & Sockets

J-EXPT J-EXPB [1)]	Utility EXPansion Interface Connector (LPC, USB, HD Audio, SMBus), available either from top (T) or bottom (B) [1)] of the board, interface to optional side board
J-HSE	High Speed Expansion Connector (4 x SATA, 4 x USB), interface to optional low profile mezzanine module or side board
J-PCIE	PCI Express® Expansion Interface Connector, interface to optional side board
J-SDVO	Digital Display Interface Connector (DisplayPort)
J1/J2	*CompactPCI* Bus 32-bit (universal V(I/O)), 33MHz, PlusIO
SODM1	204-pin DDR3 ECC Memory Module SDRAM PC3-12800 Socket (ECC SODIMM)
XDP	CPU Debug Port [1)]

[1)] Connector populated on customers request only

Pin Headers

P-FPH	Pin header suitable for Front Panel Handle switch cable harness
P-ISP	PLD glue logic device programming connector, not populated

Jumpers

DS-P	Switches to configure link width and speed on J-PCIE
P-GP	Jumper to reset UEFI BIOS Setup to EKF Factory Defaults
P-MFG	Jumper to enter Manufacturing Mode, not populated
P-RTC	Jumper to reset RTC circuitry (part of PCH), not populated

Microprocessor

The PC3-ALLEGRO is equipped with Intel® Core™ i7 or i5 3rd generation mobile ECC processor (code name Ivy Bridge). These low power processors provide integrated graphics and memory controller, which results in a very efficient platform design. The Core™ processors almost can be considered as a single-chip solution, since all functions of a typical north-bridge have been moved to the CPU.

The Core™ i7 and i5 processor family includes beside the Standard-Voltage (SV) also several Ultra Low-Voltage (ULV) and Low-Voltage (LV) processors as listed below. The processors are housed in a Micro FC-BGA package for direct soldering to the PCB, i.e. the chip cannot be removed or changed by the user.

The processors supported by the PC3-ALLEGRO are running at core clock speeds up to 2.1GHz for quad core and up to 2.5GHz on dual core devices. Due to Enhanced Intel® SpeedStep® and Intel® Turbo Boost Technology each core can decrease or increase its nominal operating frequency. The clock speed is chosen depending on the power states of the processor cores/graphics engine, the currently required performance, and the actual core temperature.

Power is applied across the *CompactPCI* connectors J1 (3.3V, 5V). The processor core voltage is generated by a switched voltage regulator, sourced from the 5V plane. The processor signals its required core voltage by 7 dedicated pins according to Intels IMVP-7 voltage regulator specification.

Intel® Core™ Processors Supported									
Processor Number	Physical Cores	Core Clock nom./max.	Cache	Gfx Clock	Junction Temp.	TDP	CPU ID	Stepping	SPEC Code
i7-3612QE	4	2.1/3.1GHz	4MB	650MHz	+105°C	35W	306A9h	E-1	SR0ND
i7-3555LE	2	2.5/3.2GHz	4MB	550MHz	+105°C	25W	306A9h	L-1	SR0T5
i7-3517UE	2	1.7/2.8GHz	4MB	350MHz	+105°C	17W	306A9h	L-1	SR0T6
i5-3610ME	2	2.7/3.3GHz	3MB	650MHz	+105°C	35W	306A9h	L-1	SR0QK

Thermal Considerations

In order to avoid malfunctioning of the PC3-ALLEGRO, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. The processor contains digital thermal sensors (DTS) that are readable via special CPU registers. DTS allows to get the temperatures of each CPU core separately.

Two further temperature sensors, located in the system hardware monitor LM87, allows for acquisition of the boards surface temperature and the thermal state of the onboard system memory channel. Beside this the LM87 also monitors most of the supply voltages. A suitable software on Microsoft Windows® systems to display both, the temperatures as well as the supply voltages, is Speedfan, which can be downloaded from the web. After installation, both temperatures and voltages can be observed permanently from the Windows® taskbar.

The PC3-ALLEGRO is equipped with a passive heatsink. Its height takes into account the 4HP limitation in mounting space of a *CompactPCI®* board. In addition, a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) is strongly recommended (>20m^3/h or 2m/s (400LFM) around the CPU slot). Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher its power consumption. For higher ambient temperatures, consider increasing the forced airflow to 3m/s (600LFM) or more.

The table showing the supported processors above give also the maximum power consumption (TDP = Thermal Design Power) of a particular processor. Fortunately, the power consumption is by far lower when executing typical Windows® or Linux tasks. The heat dissipation increases when e.g. rendering software like the Acrobat Distiller is executed.

The Core™ i7 processors support Intel's Enhanced SpeedStep® technology. This enables dynamic switching between multiple core voltages and frequencies depending on core temperature and currently required performance. The processors are able to reduce their core speed and core voltage in multiple steps down to 1200MHz (800MHz for LV/ULV processors). Additional a reduction of the graphics core clock and voltage is possible. This leads to an obvious reduction of power consumption resulting in less heating. This mode of lowering the processor core temperature is called TM2 (TM=Thermal Monitor).

Another way to reduce power consumption is to modulate the processor clock. This mode (TM1) is achieved by actuating the 'Stop Clock' input of the CPU. A throttling of 50% e.g. means a duty cycle of 50% on the stop clock input. However, while saving considerable power consumption, the data throughput of the processor is also reduced. The processor works at full speed until the core temperature reaches a critical value. Then the processor is throttled by 50%. As soon as the high temperature situation disappears the throttling will be disabled and the processors runs at full speed again.

These features are controllable by BIOS menu entries. By default the BIOS of the PC3-ALLEGRO enables mode TM2 which is the most efficient.

Main Memory

The PC3-ALLEGRO features two channels of DDR3 SDRAMs with support of ECC (Error Correction Code). One channel is realized with 18 memory devices soldered to the board (Memory Down) and delivers a capacity of up to 8GB with a clock frequency of 1600MHz (PC3-12800).

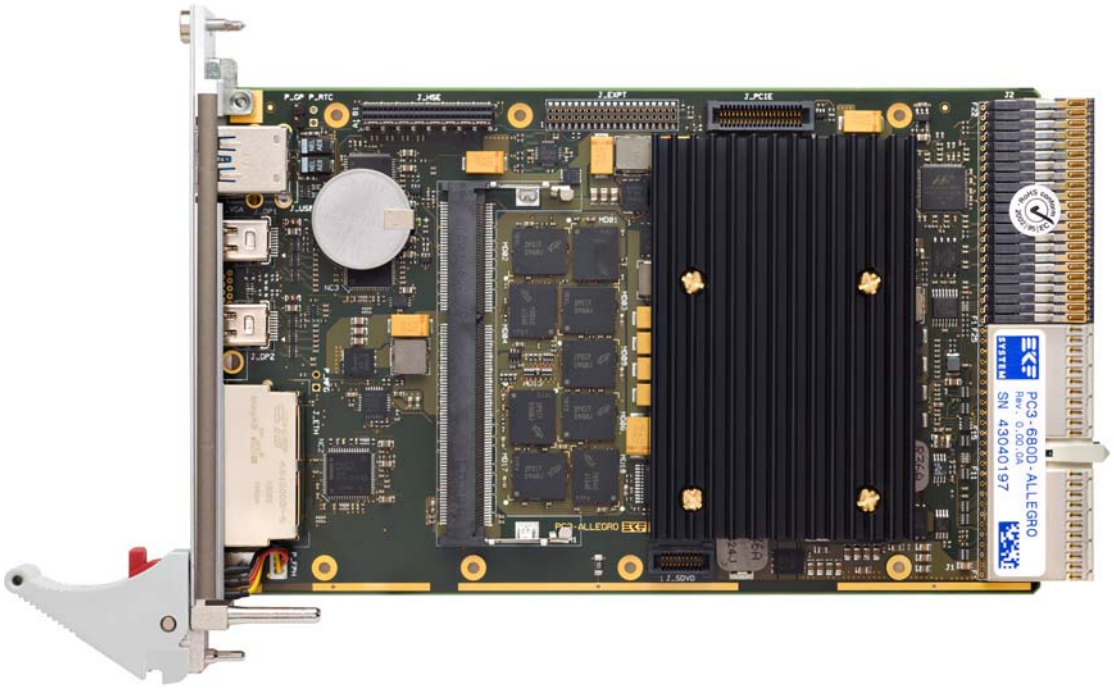
The 2nd channel provides a socket for installing a 204-pin ECC SODIMM module thus allowing a simple expansion of system memory (max. module height = 1.25 inch). Supported are unbuffered DDR3 ECC SODIMMs (72-bit) with V_{DD}=1.5V featuring on-die termination (ODT), according the PC3-12800 specification. Minimum module size is 512MB; maximum module size is 8GB. Please note that standard DDR3 SODIMMs without ECC feature do not work on PC3-ALLEGRO.

It is recommended to add a SODIMM module with same size as the Memory Down to get best performance (some of the system memory is dedicated to the graphics controller). This typically results in a size of 2x4GB of memory which is recommended to run the operating systems Windows® Vista or Windows® 7.

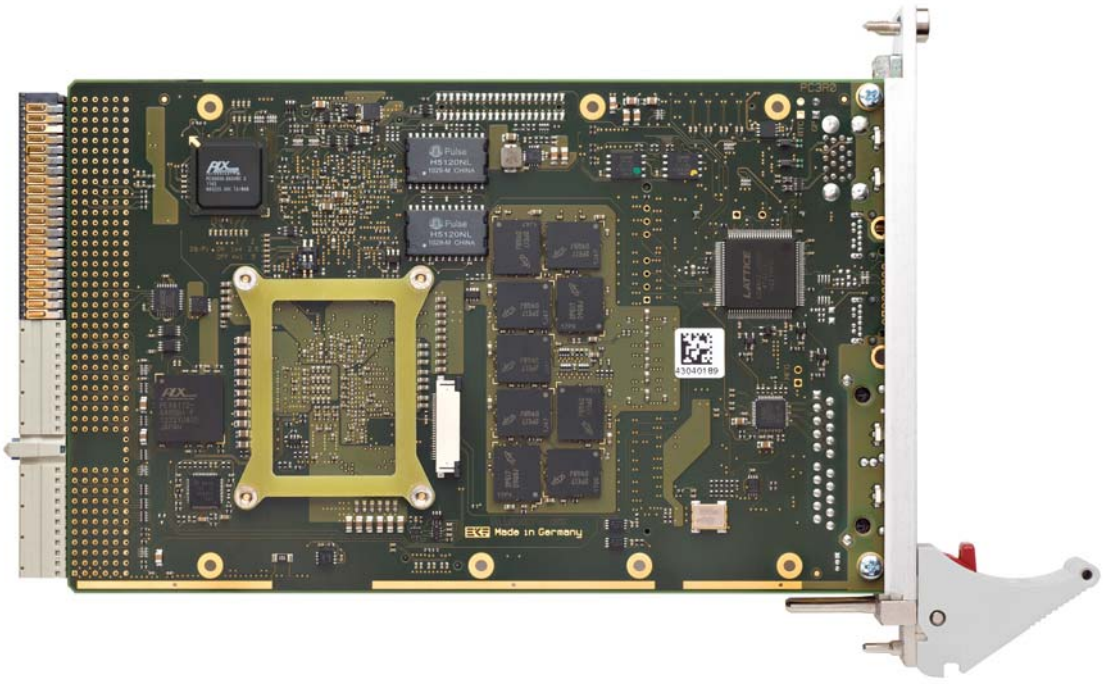
The memory controller supports symmetric and asymmetric memory organization. The maximum memory performance can be obtained by using the symmetric mode. When in this mode, the memory controller accesses the memory channels in an interleaved way. Since Core™ i7 processors support Intels Flex Memory Technology, interleaved operation isn't limited to systems using memory channels of equal capacity. In the case of unequal memory population the smaller memory channel dictates the address space of the interleaved accessible memory region. The remainder of the memory is then accessed in non-interleaved mode.

In asymmetric mode the memory always will be accessed in a non-interleaved manner with the drawback of less bandwidth. The only meaningful application of asymmetric mode is the special case when only one memory channel is populated (i.e. the SODIMM socket may be left empty).

The contents of the SPD EEPROM on the SODIMM is used by the BIOS at POST (Power-on Self Test) to get any necessary timing parameters to program the memory controller within the chipset.



Top Side Soldered Memory



Bottom Side Soldered Memory

Graphics Subsystem

The graphics subsystem is part of the Intel Core™ i7 processor and the PCH QM77. While the graphics controller is located within the Core™ i7 processor, the different interfaces like DisplayPort and VGA are moved to the PCH. The PC3-ALLEGRO offers two Mini DisplayPort (mDP) interfaces in the front panel.

Adapters to convert Mini DisplayPort to any other popular interface standard are available.

A 3rd DisplayPort is fed to the on-board connector J-SDVO. EKF expansion boards like PCS-BALLET feature the possibility to gain access to the 3rd DisplayPort interface.

As an option, the PC3-ALLEGRO can be equipped with an ordinary HD D-Sub 15-lead connector (VGA style). This connector is suitable for analog signals only. Nevertheless also flat-panel displays can be attached to the D-Sub connector but with minor reduced image quality.

Independent from the video connector actually in use, Mini DisplayPort, DVI or VGA, the VESA DDC standard is supported. This allows to read out important parameters, e.g. the maximum allowable resolution, from the attached monitor. DDC Power, +3.3V or +5V on DisplayPort or VGA connector respectively, is delivered via a resettable fuse to protect the board from an external short-circuit condition (0.5A).

Graphics drivers for the Core™ i7 can be downloaded from the Intel web site.

LAN Subsystem

The Ethernet LAN subsystem is composed of four Gigabit Ethernet ports: One Intel 82579LM Physical Layer Transceiver (PHY) using the PCH QM77 internal MAC and three Intel 82574IT Gigabit Ethernet Controllers. These devices provide also legacy 10Base-T and 100Base-TX connectivity. Two of the Ethernet ports are fed to two RJ45 jacks located in the front panel, the others are attached to the *CompactPCI®* PlusIO interface on J2. Each port includes the following features:

- One PCI Express lane per Ethernet port (250MB/s)
- 1000Base-Tx (Gigabit Ethernet), 100Base-TX (Fast Ethernet) and 10Base-T (Classic Ethernet) capability.
- Half- or full-duplex operation.
- IEEE 802.3u, 802.3ab Auto-Negotiation for the fastest available connection.
- Jumperless configuration (complete software-configurable).

Two bicoloured LEDs integrated into the dedicated RJ-45 connector in the front panel are used to signal the LAN link, the LAN connection speed and activity status. A further bicoloured LED in front panel labelled EB displays the state of the backplane network ports.

Each device is connected by a single PCI Express lane to the PCH. Their MAC addresses (unique hardware number) are stored in dedicated FLASH/EEPROM components. The Intel Ethernet software and drivers for the 82579 and 82574 is available from Intel's World Wide Web site for download.

When managing the board by Intel Active Management Technology (iAMT), the dedicated network port to do so is accessible by the RJ45 connector GbE1 (the upper port within the front panel).

Serial ATA Interface (SATA)

The PC3-ALLEGRO provides a total of eight serial ATA (SATA) ports, derived from two independent SATA controllers. Two of these ports support data transfer rates of 6Gbps (600MB/s) while all ports are capable to work with 3Gbps (300MB/s) or 1.5Gbps (150MB/s).

The SATA controller that is located within the QM77 Platform Controller Hub hold two 6Gbps and two 3Gbps ports which are fed to the high speed expansion connector J-HSE. This connector allows the installation of low profile expansion boards like C41-CFAST or C42-SATA to attach the popular CFast cards or Micro SATA SSDs (1.8-inch) respectively. Another mezzanine is the C47-MSATA, a carrier for two MSATA SSD modules, that is connected via J-HSE to the 6Gbps ports for fast data storage.

Four SATA interfaces are provided by a Marvell 88SE9230 Controller available on the Backplane connector J2. Hardware RAID configuration level 0/1/10 is supported. Please be aware that CompactPCI PlusIO Specefication does not support SATA 6G. Therefore J2 SATA channels are configured as SATA 3G.

A LED named HD located in the front panel, signals disk activity status of any of the SATA devices.

Additionally a variety of side cards is available, suitable for mounting on the PC3-ALLEGRO in a 4HP (20.32mm) distance (resulting in 8HP front panel width for the assembly). Some of these side boards can accommodate a SATA drive, e.g. a 2.5-inch SSD.

Available for download from Intel's web site are drivers for popular operating systems, e.g. Windows® XP, Windows® Vista, Windows® 7 and Linux.

To manage the RAID configuration of the 88SE9230 a Windows® application is provided by Marvell that can be downloaded from EKF's website.

PCI Express® Interface

The PC3-ALLEGRO is provided with several PCI Express (PCIe) lanes for I/O expansion. Four PCI Express Gen 2 lanes (5GT/s), originating from the QM77, are available at the backplane connector J2. Another four PCI Express lanes are provided by the Intel Core™ i7 processor to the J-PCIE connector. A small DIP switch (DS-P) located on the backside of the board are used to configure different lane widths to each of both downstream interfaces and to choose the interface transfer rate. Possible settings are

- Single link x 4 lanes to J-PCIE
- Four links x 1 lane to J-PCIE
- 2.5GT/s or 5GT/s transfer speed

See section “Configuration PCI Express Switch (DS-P)” for details.

Universal Serial Bus (USB)

The PC3-ALLEGRO is provided with twelve USB ports. All of them are USB 2.0 capable, but two ports, routed to front panel connectors, are also supporting the USB 3.0 SuperSpeed standard.

The USB 2.0 interfaces are distributed to the front panel (two ports), two to the expansion board interface connectors J-EXP, four to the high speed expansion connector J-HSE, and four ports are available across the backplane connector J2.

The front panel USB connectors can source a minimum of 1.5A/5V each, over-current protected by two electronic switches. Protection for the USB ports on the expansion interfaces and on the J2 PlusIO connector is located on expansion boards. The USB xHCI and two EHCI controllers handling the USB port operation at SuperSpeed, high-speed, full-speed and low-speed are integrated into the QM77 PCH.

Utility Interfaces

Besides the high speed mezzanine interface connectors J-HSE and J-PCIE, the PC3-ALLEGRO is provided with the utility interface expansion connector socket J-EXP. This connector comprises several interfaces, which may be useful for system expansion on mezzanine cards, as an option:

- HD Audio
- LPC (Low Pin Count)
- SMBus
- 2 x USB

The SMBus is controlled by the QM77 platform controller hub. The SMBus signal lines on the J-EXP utility expansion connector can be switched on/off under software control (PCH GPIO) in order to isolate external components in case of an I^2C address conflict.

The HD Audio port requires an additional audio codec, as provided e.g. on the PCS-BALLET side card.

The LPC bus presents an easy way to add legacy interfaces to the system. EKF offers a variety of mezzanine expansion boards (side cards), to be attached on top of the PC3-ALLEGRO, featuring all classic Super-I/O functionality, for example the PCS-BALLET or the CCO-CONCERT. Access to the connectors PS/2 (mouse, keyboard), COM, USB and audio in/out is given directly from the front panel.

Real-Time Clock

The PC3-ALLEGRO has a time-of-day clock and 100-year calendar, integrated into the QM77 PCH. A battery on the board keeps the clock current when the computer is turned off. The PC3 uses a BR2032 lithium battery soldered in the board, giving an autonomy of more than 5 years. Under normal conditions, replacement should be superfluous during lifetime of the board.

In applications were the use of a battery is not permitted, a SuperCap can be stuffed instead of the battery.

SPI Flash

The BIOS and iAMT firmware is stored in flash devices with Serial Peripheral Interface (SPI). Up to 16MByte of BIOS code, firmware and user data may be stored nonvolatile in these SPI Flashes.

The SPI Flash contents can be updated by a DOS or Linux based tool. This program and the latest PC3-ALLEGRO BIOS binary are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g. caused by a power interruption, the PC3-ALLEGRO may no more be operable. In this case you would possibly have to send in the board, because the Flash device is directly soldered to the PCB and cannot be changed by the user.

Reset

The PC3-ALLEGRO is provided with several supervisor circuits to monitor supply rails like the CPU core voltage, 1.5V, 3.3V or 5V. This circuitry is responsible also to generate a clean power-on reset signal.

To force a manual board reset, the PC3-ALLEGRO offers a small tactile switch within the front panel. This push-button is indent mounted and requires a tool, e.g. a pen to be pressed, preventing from being inadvertently activated.

The ejector within the front panel contains a micro switch that is used to generate a power button event. This is done by pushing the red button of the ejector until the handle unlocks without ejecting the board. Immediately after that push up the ejector back to its original position (the red button jumps up as well). Animated GIF: www.ekf.com/c/ccpu/img/reset_400.gif

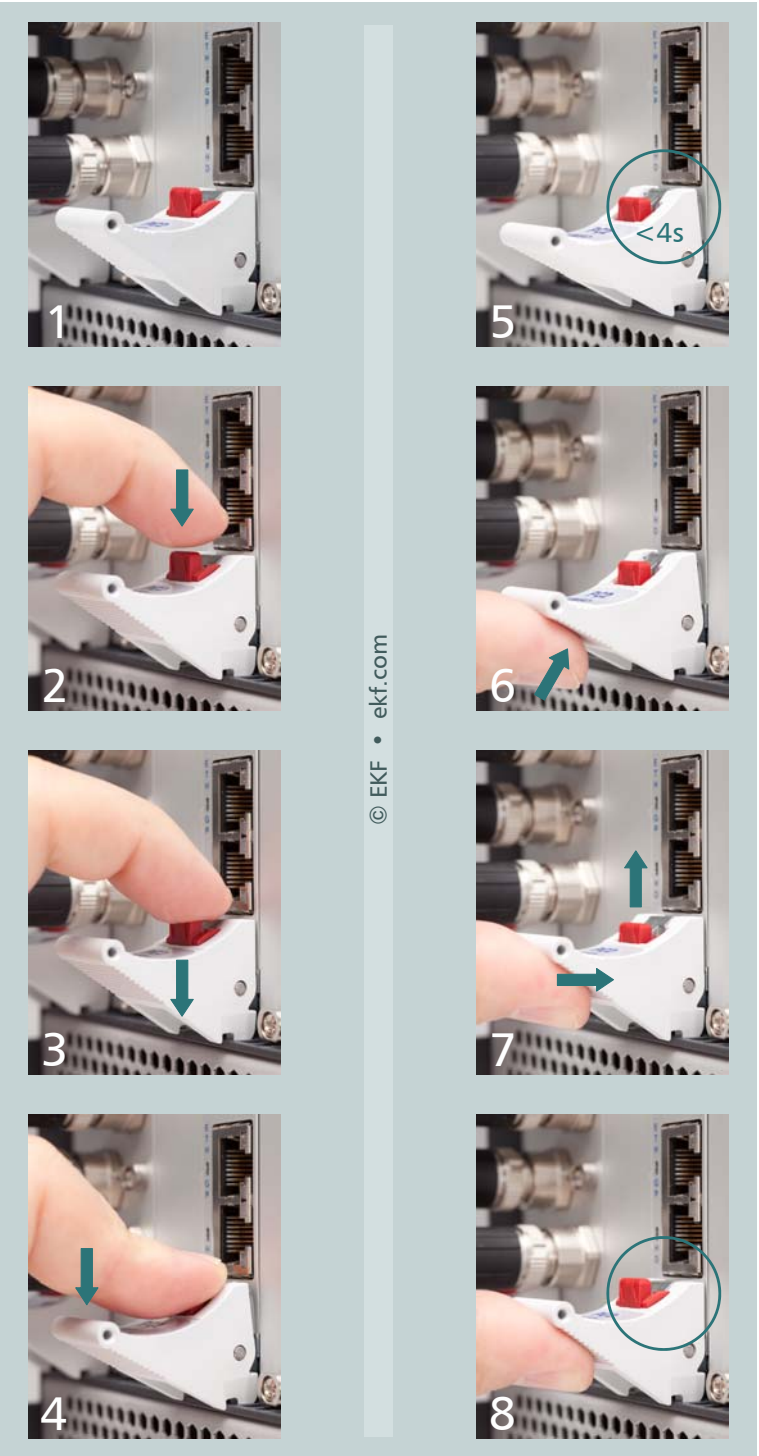
NOTE: To prevent the board to cause a power button override, the handle should be closed immediately after unlocking the front panel handle. A power button override is triggered by opening the front panel handle for at least 4 seconds, which results in bringing the board to power state S5. In case of entering this state, unlock and lock the front panel handle a 2nd time to reenter normal power state S0 again. See also section 'PG (Power Good) LED' to see how the PC3-ALLEGRO indicates the different power states.

WARNING: The PC3-ALLEGRO will enter the power state S5 if the front panel handle is not closed properly when the system powers up. An open handle is signalled by a yellow blinking 'PG LED'.

The manual reset push-button and the power button functionality of the front panel handle could be passivated by BIOS settings.

An alternative (and recommended) way to generate a system reset is to activate the signal PRST# located on *CompactPCI* connector J2 pin C17. Pulling this signal to GND will have the same effect as to push the tactile reset switch.

The healthy state of the PC3-ALLEGRO is indicated by the LED PG (Power Good) located in the front panel. This bicoloured LED signals different states of the board (see section below). As soon as this LED begins to lite green, all power voltages are within their specifications and the reset signal has been deasserted.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Watchdog

An important reliability feature is a software programmable watchdog function. The PC3-ALLEGRO contains two of these watchdogs. One is part of the QM77 PCH and also known as TCO Watchdog. A detailed description is given in the QM77 data sheet. Operating systems like Linux offer a driver interface to the TCO watchdog.

The behaviour of the 2nd watchdog is defined within a PLD of the PC3, which activates/deactivates the watchdog and controls its time-out period. The time-out delay is adjustable in the steps 2, 10, 50 and 255 seconds. After alerting the WD and programming the time-out value, the related software (e.g. application program) must trigger the watchdog periodically. For details on programming the watchdog see section "Board Control and Status Register (BCSR)".

This watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. The watchdog is activated on the first trigger request. If the duration between two trigger requests exceeds the programmed period, the watchdog times out and a full system reset will be generated. The watchdog remains in the active state until the next system reset. There is no way to disable it once it has been put on alert, whereas it is possible to reprogram its time-out value at any time.

Front Panel LEDs

The PC3-ALLEGRO is equipped with four LEDs which can be observed from the front panel. Three of these LEDs are labelled according to their primary meaning, but should be interpreted altogether for system diagnosis:

LED			Status
PG Green/Red	GP Green/Red	HD Green/Red	
OFF	GREEN	GREEN	Sleep State S5 (Soft Off)
OFF	GREEN	OFF	Sleep State S4 (Suspend to Disk/Hibernate)
OFF	OFF	GREEN	Sleep State S3 (Suspend to RAM/Standby)
GREEN	RED BLINK	X	After Reset
GREEN	X	X	Board Healthy and in S0 State
YELLOW BLINK	X	X	Front panel handle is unlocked
RED	X	X	Hardware Failure - Power Fault
RED BLINK	X	X	Software Failure

PG (Power Good) LED

The PC3-ALLEGRO offers a bicolour LED labelled PG located within the front panel. After system reset, this LED defaults to signal different power states:

- Off Sleep state S3, S4 or S5
- Green Healthy
- Yellow blink Front panel handle open
- Red steady Hardware failure
- Red blink Software failure

To enter the PG LED state *Software Failure,* the bit PGLED in the board control register CTRLL_REG must be set. The PG LED remains in this red blinking state until this bit is cleared. After that it falls back to its default function.

GP (General Purpose) LED

This programmable bicolour LED can be observed from the PC3-ALLEGRO front panel. The status of the red part within the LED is controlled by the GPIO18 of the PCH QM77. Setting GPIO18 to "1" will switch on the red LED. Turning on or off the green LED is done by setting the bit GPLED in the board control register CTRLH_REG.

The GP LED is not dedicated to any particular hardware or firmware function with exception of special power states of the LED PG as described above. Nevertheless, a red blinking GP LED is an indication that the BIOS code couldn't start.

While the CPU card is controlled by the BIOS firmware, the GP LED is used to signal board status information during POST (Power On Self Test). After successful operating system boot, the GP LED may be freely used by customer software. For details please refer to www.ekf.com/p/pc3/firmware/biosinfo.txt.

HD (Hard Disk Activity) LED

The PC3-ALLEGRO offers a bicoloured LED marked as HD placed within the front panel. This LED, when blinking green, signals activity on any device attached to the SATA ports of the Intel® QM77 Panther Point Platform Controller Hub (PCH). Blinking yellow signals activity on any device attached to the SATA ports of the Marvell 88SE9230 SATA RAID Controller.

As previously described, the green part of this LED may change its function dependent on the state of the LED PG.

EB (Ethernet Backplane) LED

To monitor the link status and activity on both Ethernet ports attached to the backplane via the *CompactPCI*® Serial connector P6 a single bicoloured LED is provided in the front panel. The states are decoded as follows:

1_ETH	2_ETH	LED EB
no link	no link	OFF
link	no link	GREEN
no link	link	YELLOW
link	link	GREEN/YELLOW

Blinking of the LED EB in the appropriate colour means that there is activity on the port.

Hot Swap Detection

The CompactPCI® specification added the signal ENUM# to the PCI bus to allow board hot swapping. This signal is routed to a GPIO (GPIO3 QM77 PCH) . An interrupt can be requested, if ENUM# changes, caused by insertion or removal of a peripheral board.

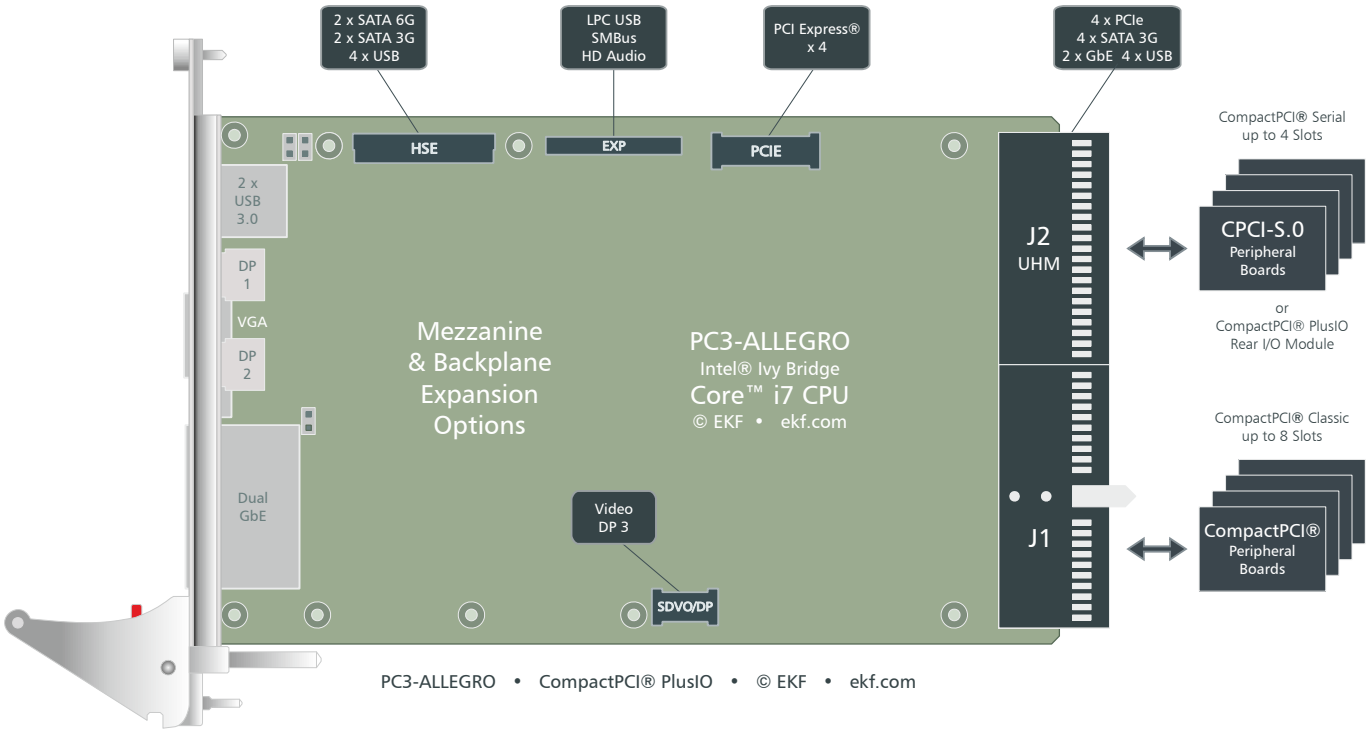
Note that the PC3-ALLEGRO itself is not a hot swap device, because it makes no sense to remove the system controller from a CompactPCI® system. However, it is capable to recognize the hot swap of peripheral boards and to start software that is performing any necessary system reconfiguration.

Power Supply Status (DEG#, FAL#)

Power supply failures may be detected before the system crashes down by monitoring the signals DEG# or FAL#. These active low lines are additions to the CompactPCI® specification and may be driven by the power supply. DEG# signals the degrading of the supply voltages, FAL# there possible failure. On the PC3-ALLEGRO DEG# is tied to VCC and FAL# is routed to QM77 PCH GPIO4.

Mezzanine Side Board Options

The PC3-ALLEGRO is provided with several stacking connectors for attachment of a mezzanine expansion module (aka side board), suitable for a variety of readily available mezzanine cards (please refer to www.ekf.com/c/ccpu/mezz_ovw.pdf for a more comprehensive overview). EKF furthermore offers custom specific development of side boads (please contact sales@ekf.de).



Most mezzanine expansion modules require an assembly height of 8HP in total, together with the CPU carrier board (resulting from two cards at 4HP pitch each). In addition, cropped low profile mass storage mezzanine modules can be attached to J-HSE, which maintain the 4HP envelope, for extremely compact systems. Furthermore these small size modules may be combined with the full-size expansion boards (that means an assembly comprised of 3 PCBs).

PC3-ALLEGRO w. PCL-CAPELLA Side Card 8HP Assembly

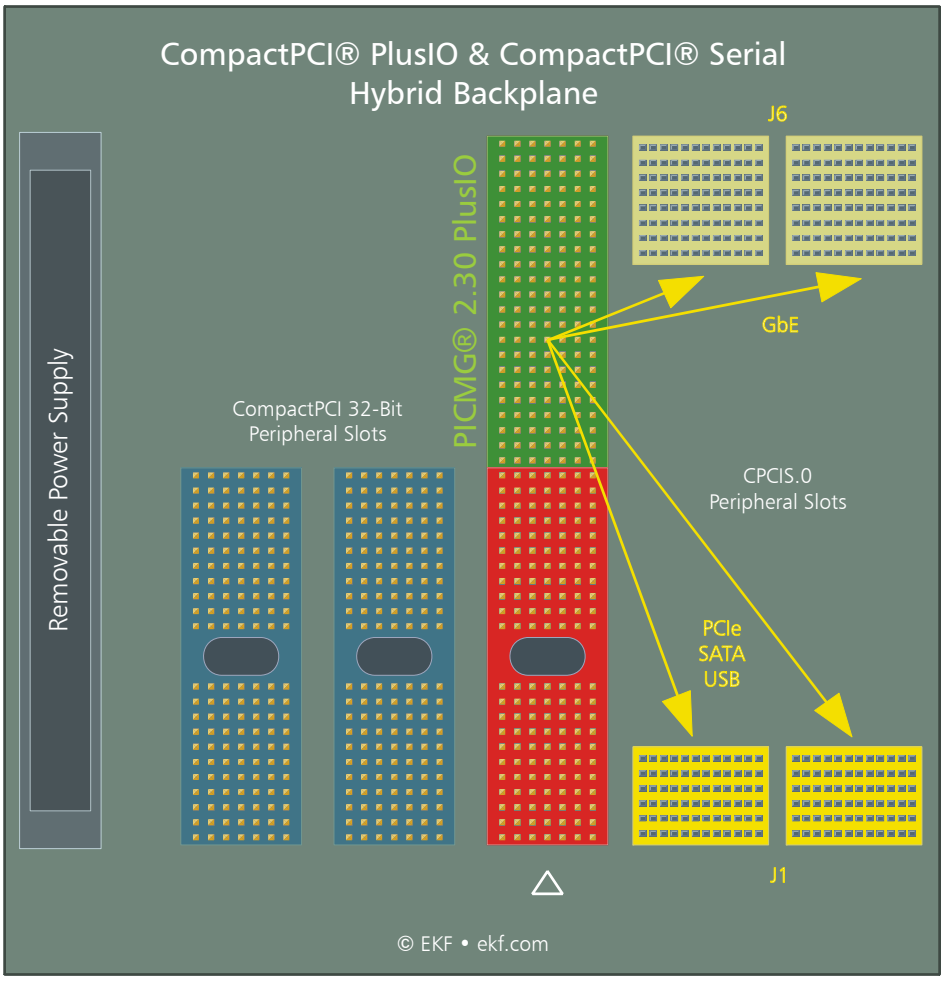
Related Documents Mezzanine Modules and Side Cards	
C40 ... C47 Series Mezzanine Storage Modules	www.ekf.com/c/ccpu/c4x_mezz_ovw.pdf
PCL-CAPELLA Mezzanine Side Card	www.ekf.com/p/pcl/pcl.html
PCS-BALLET Mezzanine Side Card	www.ekf.com/p/pcs/pcs.html

CompactPCI® PlusIO

CompactPCI® PlusIO (PICMG® 2.30) is a standard for rear I/O across J2. High speed signal lines (PCI Express®, SATA, Gigabit Ethernet and USB) are passed from the PC3-ALLEGRO through the special UHM J2 connector to the backplane, for usage either with a PlusIO rear I/O transition module, or CompactPCI® Serial card slots.

CompactPCI® Serial (PICMG® CPCIS.0) defines a completely new card slot, based on PCI Express®, SATA, Gigabit Ethernet and USB serial data lines. On a hybrid backplane, both card styles can reside, CompactPCI® and CompactPCI® Serial, with the PC3-ALLEGRO in the middle as controller for both backplane segments.

The PC3-ALLEGRO can be used in any system with a CompactPCI® PlusIO backplane according to the PICMG® 2.30 specification. Hybrid backplanes allow the configuration of systems with CompactPCI® Serial slots in addition to classic CompactPCI® boards.



Sample Small Systems Hybrid Backplane

Warning: Do not operate the PC3-ALLEGRO in systems with a 64-bit CompactPCI® backplane. The J2/P2 pin assignments of a 64-bit CPCI backplane differ substantially from a CompactPCI® PlusIO backplane, which may result in a short circuit situation.

For use with a 64-bit CompactPCI® backplane special versions are available on request. 32-bit operation is supported only. The use of 64-bit CompactPCI® peripheral boards may cause problems.

PC1-GROOVE as System Controller in a Hybrid System

CompactPCI® PlusIO Racks Available

As an alternate, the PC3-ALLEGRO can be combined with a CompactPCI® PlusIO rear I/O transition module, such as the PR1-RIO, which is provided with I/O connectors (on-board and back-panel) for all high speed signals.

PR1-RIO • Rear I/O Transition Module

Related Documents Mezzanine Modules and Side Cards	
C4x Series Mezzanine Storage Modules	www.ekf.com/c/ccpu/c4x_mezz_ovw.pdf
Mezzanine Modules Overview	www.ekf.com/c/ccpu/mezz_ovw.pdf
The EKF Mezzanine Module Concept	www.ekf.com/c/ccpu/cpci_mezzanine_evolution.pdf

J-EXP	
I/F Type	Controller
LPC (Low Pin Count)	CPU
HD Audio	CPU
SMBus	CPU (buffered)
2 x USB 2.0	PCH

J-HSE	
I/F Type	Controller
SATA1, SATA4	PCH 3GT/s
SATA2, SATA3	PCH 6GT/s
4 x USB 2.0	USB Hub

J-PCIE	
I/F Type	Controller
PCI Express®	PE Switch

Related Documents *CompactPCI®* Serial	
CompactPCI® PlusIO & Serial Overview	www.ekf.com/s/smart_solution.pdf
CompactPCI® Serial Home	www.ekf.com/s/serial.html
CompactPCI® PlusIO Home	www.ekf.com/p/plus.html

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system

- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related *CompactPCI®* slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- Unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Recommended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

Replacement of the Battery

When your system is turned off, a battery maintains the voltage to run the time-of-day clock and to keep the values in the CMOS RAM. The battery should last during the lifetime of the PC3-ALLEGRO. For replacement, the old battery must be desoldered, and the new one soldered. We suggest that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced or shorted. Replace only with the same or equivalent type. Do not expose a battery to fire.

Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. Several devices are part of the processor and platform controller hub QM77.

Bus #	Device #	Function #	Vendor ID	Device ID	Description
0	0	0	0x8086	0x0154	Processor Host Bridge/DRAM Controller
0	1	0	0x8086	0x0151	Processor PCI Express Controller
0	1	1	0x8086	0x0155	Processor PCI Express Controller
0	1	2	0x8086	0x0159	Processor PCI Express Controller
0	6	0	0x8086	0x015D	Processor PCI Express Controller
0	2	0	0x8086	0x0166	Processor Integrated Graphics Device
0	20	0	0x8086	0x1E31	USB xHCI Controller
0	22	0	0x8086	0x1E3A	Intel ME Interface #1
0	22	1	0x8086	0x1E3B	Intel ME Interface #2
0	22	2	0x8086	0x1E3C	Intel ME IDE Redirection
0	22	3	0x8086	0x1E3D	Intel ME Keyboard Text Redirection
0	25	0	0x8086	0x1502	PCH Gigabit LAN NC1 (82579LM)
0	26	0	0x8086	0x1E2D	USB EHCI Controller #2
0	27	0	0x8086	0x1E20	Intel High Definition Audio Controller
0	28	0-7	0x8086	0x2448	PCH PCI Express Port 1-8
0	29	0	0x8086	0x1E26	USB EHCI Controller #1
0	31	0	0x8086	0x1E55	LPC Bridge
0	31	2	0x8086	0x1E01 0x1E03 0x282A 0x1E07	SATA: Non-AHCI/RAID (Ports 0-3) [1] SATA: AHCI Mode [1] SATA: Intel Rapid Storage Tech. RAID Mode [1] SATA: RAID Mode Capable [1]
0	31	3	0x8086	0x1E22	SMBus Controller
0	31	5	0x8086	0x1E09	SATA: Non-AHCI/RAID (Ports 4/5)
0	31	6	0x8086	0x1E24	Thermal Controller
1 [2]	00	0	0x10B5	0x8614	PCIe Switch Root Port (PEX8608)
2 [2]	01,05,07,09	0	0x10B5	0x8614	PCIe Switch Downstream Ports (PEX8608)
7 [2]	0	0	0x1B4B	0x9230	Marvell 9230 SATA Controller
10 [2]	00	0	0x8086	0x10D3	Ethernet Controller NC2 (82574IT)
11 [2]	00	0	0x8086	0x10D3	Ethernet Controller NC3 (82574IT)
12 [2]	00	0	0x8086	0x10D3	Ethernet Controller NC4 (82574IT)

[1] Depends on BIOS settings. [2] Bus number can vary depending on the PCI enumeration schema implemented in BIOS.

Local SMB Devices

The PC3-ALLEGRO contains devices that are attached to the System Management Bus (SMBus). These are the SPD EEPROMs for the on-board memory or the possibly plugged SODIMM, a general purpose serial EEPROM, a supply voltage/temperature controlling device and a set of board control and status registers. Additional devices may be connected to the SMBus via the *CompactPCI*® Serial backplane signals I^2C_SCL (P1 B2) and I^2C_SDA (P1 B3), or pins 29/30 of the mezzanine expansion connector J-EXP.

Address	Description
0x58	Hardware Monitor/Memory Down Temperature Sensor (LM87)
0x5C	Board Control/Status
0xA0	SPD of On-board Memory
0xA4	SPD of SODIMM
0xAE	General Purpose EEPROM

Hardware Monitor LM87

Attached to the SMBus, the PC3-ALLEGRO is provided with a hardware monitor (LM87). This device is capable to observe the board and on-board memory temperatures, as well as several supply voltage rails with a resolution of 8 bit. The following table shows the mapping of the voltage inputs of the LM87 to the corresponding supply voltages of the PC3-ALLEGRO:

Input	Source	Resolution [mV]	Register
AIN1	Processor Core Voltage	9.8	0x28
AIN2	Graphics Core Voltage	9.8	0x29
VCCP1	+1.5V	14.1	0x21
VCCP2/D2-	+1.8V	14.1	0x25
+2.5V/D2+	+1.05V	13	0x20
+3.3V	+3.3V	17.2	0x22
+5V	+5V	26	0x23
+12V	+10V	62.5	0x24

Beside the continuous measuring of temperatures and voltages the LM87 may compare these values against programmable upper and lower boundaries. As soon as a measurement violates the allowed value range, the LM87 can request an interrupt via the GPI13 input of the QM77 PCH (which may result in a system management interrupt).

Board Control and Status Registers

A set of board control and status registers allow to program special features on the PC3-ALLEGRO:

- Assert a full reset
- Control activity of front panel reset and power event button
- Program time-outs and trigger a watchdog
- Get access to two LEDs in the front panel
- Get power fail and watchdog status of last board reset

The register set consists of five registers located on the SMBus at Device ID=0x5c on the following addresses:

- 0xA0: CMD_CTRL0_WR: Write to Control Register 0 (Write-Only)
- 0xA1: CMD_CTRL0_RD: Read from Control Register 0 (Read-Only)
- 0xB0: CMD_STAT0_WR: Write to Status Register 0 (Write-Clear)
- 0xB1: CMD_STAT0_RD: Read from Status Register 0 (Read-Only)
- 0xB2: CMD_STAT1_WR: Write to Status Register 1 (Write-Clear)
- 0xB3: CMD_STAT1_RD: Read from Status Register 1 (Read-Only)
- 0xC1: CMD_PLDREV_RD: Read from PLD Revision Register (Read-Only)

To prevent misfunction accesses to the registers should be done by SMBus “Byte Data” commands. Further writes to read-only or reads to write-only registers should be omitted.

Write/Read Control Register 0

Write: SMBus Address 0xA0 Default after reset: 0x00

Read: SMBus Address 0xA1

Bit	Description CMD_CTRL0
7	**GPLED** 0=Green part of the front panel LED GP is off (Default) 1=Green part of the front panel LED GP is on
6	**FPDIS** 0=Enable the power event button within the front panel handle (Default) 1=Disable the power event button within the front panel handle
5	**FRDIS** 0=Enable the system reset button within the front panel (Default) 1=Disable the system reset button within the front panel
4:3	**WDGT0:WDGT1** Maximum Watchdog retrigger time: 0:0 2 sec 1:0 10 sec 0:1 50 sec 1:1 250 sec
2	**WDGTRG** Retrigger Watchdog. Any change of this bit will retrigger the watchdog. After a system reset the watchdog is in an inactive state. The watchdog is armed on the 1st edge of this bit.
1	**PGLED** 0=Red part of the front panel LED PG is off (Default) 1=Red part of the front panel LED PG is blinking
0	**SRES** 0=Normal operation (Default) 1=A full system reset is performed

Read/Clear Status Register 0

Write: SMBus Address 0xB0
Read: SMBus Address 0xB1

Bit	Description CMD_STAT0
7	**PF18S** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.8S voltage regulator
6	**PF15S** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.5S voltage regulator
5	**RESERVED** Always read as 0
4	**PFVSA** 0=Normal operation 1=Last system reset may be caused by a power failure of the CPU +VCC_SA voltage regulator
3	**PF105L** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.05LAN voltage regulator
2	**PF105S** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.05S voltage regulator
1	**PFVRG** 0=Normal operation 1=Last system reset may be caused by a power failure of the CPU +VCC_AXG voltage regulator
0	**PFVRC** 0=Normal operation 1=Last system reset may be caused by a power failure of the CPU +VCC_CPU voltage regulator

The bits in this register are sticky, i.e. their state will be kept even if a system reset occurs. To clear the bits a write to the register with arbitrary data may be performed.

Read/Clear Status Register 1

Write: SMBus Address 0xB2
Read: SMBus Address 0xB3

Bit	Description CMD_STAT1
7	**RESERVED** Always read as 0
6	**WDGRST** 0=Normal operation 1=Last system reset may be caused by a watchdog time-out
5	**WDGHT** 0=Normal operation 1=The watchdog already has elapsed half of its time-out period
4	**PF12A** 0=Normal operation 1=Power failure on the +12V voltage rail
3	**PF133S** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.05S or +V3.3S voltages
2	**PF133M** 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.05M or +V3.3M voltages
1	**RESERVED** Always read as 0
0	**RESERVED** Always read as 0

Except of WDGHT the bits in this register are sticky, i.e. theire state will be kept even if a system reset occurs. To clear the bits a write to the register with arbitrary data may be performed.

Read PLD Revision Register

Write: Not allowed

Read: SMBus Address 0xC1

Bit	Description CMD_PLDREV
7:0	**PLDREV** Read PLD Revison Number

GPIO Usage

GPIO Usage QM77 PCH

GPIO Usage QM77 PCH				
GPIO	Type	Tol.	Function	Description
GPIO 0	I	3.3V	THRM_ALERT#	Monitoring of processor PROCHOT#
GPIO 1	I	3.3V	EXP_SMI#	Expansion Interface SMI Request (J-EXP Pin 15)
GPIO 2	I	5V	CPCI_INTP	CompactPCI Interrupt Request Line INTP
GPIO 3	I	5V	CPCI_ENUM#	CompactPCI System Enumeration Line ENUM#
GPIO 4	I	5V	CPCI_PS_FAL_ON#	CompactPCI Power Failure Line FAL# / PS_ON#
GPIO 5	I	5V	PM_MEMTS#	Memory Thermal Sensor
GPIO 6	-	3.3V	-	Not used, pulled to GND
GPIO 7	I	3.3V	CPCI_SYSEN_#	Sense CPCI System Slot Enable
GPIO 8	-	3.3V	-	Not used, pulled to +V3.3A/
GPIO 9	I	3.3V	USB_HSE_OC5#	USB HSE Port #2 Overcurrent Detect
GPIO 10	O	3.3V	USB_OC6#	USB HSE Port #3 or #4 Overcurrent Detect
GPIO 11	I	3.3V	GP_JUMP#	Reset UEFI BIOS Setup to Factory Defaults, Jumper P-GP
GPIO 12	O	3.3V	NC1_ENABLE	Enable Ethernet Controller NC2
GPIO 13	I	3.3V	HM_INT#	Hardware Monitor LM87 Interrupt Line
GPIO 14	I	3.3V	USB_OC7#	USB J-EXP Port 1 or 2 Overcurrent Detect
GPIO 15	-	3.3V	-	Not used, pulled to +V3.3A
GPIO 16	O	3.3V	MODE_DP_SDVO#	Switch Mode of J-SDVO Connector LOW: J-SDVO in SDVO Mode HIGH: J-SDVO in DisplayPort Mode
GPIO 17	-	3.3V	-	Not used, pulled to GND
GPIO 18	O	3.3V	GP_LED_RED	General Purpose Red LED Control (via PLD)
GPIO 19	-	3.3V	-	Not used, pulled to +V3.3A
GPIO 20	O	3.3V	SE_SYS_WP	General Purpose Serial EEPROM Write Protection
GPIO 21	-	3.3V	-	Not used, pulled to +V3.3A
GPIO 22	O	3.3V	SGPIO_CLOCK	Serial GPIO Bus CLOCK
GPIO 23	-	3.3V	-	Not used, internally pulled up
GPIO 24	O	3.3V	USB_POWEN1#	USB Front Panel Right Port Power Enable
GPIO 25	O	3.3V	CLKOE_2J2	J2 PCIe2 clk enable, pulled to +V3.3A
GPIO26	O	3.3V	CLKOE_1J2	J2 PCIe1 clk enable, pulled to +V3.3A
GPIO 27	O	3.3V	USB_POWEN2#	USB Front Panel Left Port Power Enable
GPIO 28	-	3.3V	-	Not used, pulled to +V3.3A
GPIO 29	-	3.3V	-	Fixed to chipset internal function
GPIO 30-32	-	3.3V	-	Not used, pulled to +V3.3A
GPIO 33	-	3.3V	-	Not used

GPIO Usage QM77 PCH				
GPIO	Type	Tol.	Function	Description
GPIO 34	O	3.3V	EXP_SMB_EN	Connect SMBus on J-EXP to local SMBus LOW: J-EXP disconnected from SMBus HIGH: J-EXP connected to SMBus
GPIO 35	I	3.3V	CPCI_SMB_EN	Connect SMBus on CPCI to local SMBus LOW: CPCI Backplane disconnected from SMBus HIGH: CPCI Backplane connected to SMBus
GPIO36-37	-	3.3V	-	Not used, pulled to GND
GPIO 38	O	3.3V	SGPIO_LOAD	Serial GPIO Bus LOAD (Backplane J2)
GPIO 39	O	3.3V	SGPIO_OUT	Serial GPIO Bus DATAOUT (Backplane J2)
GPIO 40	I	3.3V	USB_OC1#	USB Front Panel Right Port Overcurrent Detect
GPIO 41	O	3.3V	ENABLE_NC3	Enable Ethernet Controller NC3
GPIO 42	O	3.3V	ENABLE_NC4	Enable Ethernet Controller NC4
GPIO 43	I	3.3V	USB_OC4#	USB J-HSE Port 1 Overcurrent Detect
GPIO 44	-	3.3V	-	Not used, pulled to GND
GPIO 45	O	3.3V	CLKOE_4J2	J2 PCIe4 clk enable, pulled to +V3.3A
GPIO 46	-	3.3V	-	Not used, pulled to GND
GPIO 47	O	3.3V	CLKOE_3J2	J2 PCIe3 clk enable, pulled to +V3.3A
GPIO 48-49	-	3.3V	-	Not used, pulled to GND
GPIO 50-52	-	3.3V	-	Not used, pulled to +V3.3S
GPIO 53	O	3.3V	CPCI_CLKBUF_EN	Enable CompactPCI Clock Buffer
GPIO 54	-	3.3V	-	Not used, pulled to +V3.3S
GPIO 55	O	3.3V	ENABLE_NC2	Enable Ethernet Controller NC2
GPIO 56	-	3.3V	-	Not used, pulled to GND
GPIO 57	O	3.3V	CPCI_INTS	LOW: Isolate SERIRQ from CPCI_INTS HIGH: Connect SERIRQ to CPCI_INTS
GPIO 58	-	3.3V	-	Not used, pulled to +V3.3A
GPIO 59	I	3.3V	USB_OC0#	USB Front Panel Right Port Overcurrent Detect
GPIO 60	-	3.3V	-	Not used, pulled to +V3.3A
GPIO 61-62	-	3.3V	-	Not used
GPIO 63	O	3.3V	N/A	Multiplexed with chipset internal function
GPIO 64-67	I		HWREV	PCB Revision Code HW_REV[2:0]: GPIO[67/66/64] 000 001 010 ... 100 ... 111 Revision 0 1 2 4 7
GPIO65	O	3.3V	CLK_14_EXP	Used as 14MHz Clock
GPIO 66	I	3.3V	HWREV	Used as HW_REV[1], see GPIO64
GPIO 67	I	3.3V	HWREV	Used as HW_REV[2], see GPIO64
GPIO68-71	I	N/A	N/A	Not used
GPIO 72	-	3.3V	-	Not used, pulled to +V3.3A
GPIO 73	I	3.3V	NC1_CLKREQ_#	Clock Enable Ethernet Controller NC1
GPIO 74-75	-	3.3V	-	Not used, pulled to +V3.3A

Configuration Jumpers

Configuration PCI Express Switch (DS-P)

The link width and transfer rate of the PCI Express interfaces attached to the local expansion connector P-PCIE is configurable by two DIP switches (DS-P) located on the backside of the PC3-ALLEGRO. Note that changes in PCIe link configuration are honoured by the PC3-ALLEGRO not before a system reset was performed.

DS-P

DS-P		PCIe Link Width	
1	2	PCIe Switch Upstream	J-PCIE
OFF	OFF	4 Lanes @ 5GT/s	4 Links x 1 Lane @ 5GT/s
ON	OFF	4 Lanes @ 5GT/s	1 Link x 4 Lanes @ 5GT/s
OFF	ON	4 Lanes @ 2.5GT/s	4 Links x 1 Lane @ 2.5GT/s
ON	ON	4 Lanes @ 2.5GT/s	1 Link x 4 Lanes @ 2.5GT/s

[1)] Consists to the non fat pipe slots, generally periphery slots 3 to 6.

When the port on J-PCIE is configured as single link, the PCIe switch may size down the link width to x2 or x1 by auto-negotiation.

The following table shows the factory settings of DS-P with different side boards mounted to the PC3-ALLEGRO:

Side Board	DS-P		PCIe Link Width
	1	2	J-PCIE
None	OFF	OFF	4 Links x 1 Lane @ 5GT/s
CCI-RAP	OFF	OFF	4 Links x 1 Lane @ 5GT/s
CCK-MARIMBA	ON	OFF	1 Link x 4 Lanes @ 5GT/s
CCL-CAPELLA	ON	OFF	1 Link x 4 Lanes @ 5GT/s
CCO-CONCERT	OFF	ON	4 Links x 1 Lane @ 2.5GT/s
PCS-BALLET	OFF	OFF	4 Links x 1 Lane @ 5GT/s

Loading UEFI BIOS Setup Defaults (P-GP)

The jumper P-GP may be used to reset the UEFI BIOS configuration settings to a default state. The UEFI BIOS on PC3-ALLEGRO stores most of its settings in an area within the BIOS flash, e.g. the actual boot devices. Using the jumper P-GP is only necessary, if it is not possible to enter the setup of the BIOS. To reset the settings mount a jumper on P-GP and perform a system reset. As long as the jumper is stuffed the BIOS will use the default configuration values after any system reset. To get normal operation again, the jumper has to be removed.

P-GP

P-GP	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	BIOS configuration reset performed

[1)] This setting is the factory default

Manufacturer Mode Jumper (P-MFG)

The jumper P-MFG is used to bring the board into the manufacturer mode. This is necessary only on board production time and should not used by customers. For normal operation the jumper should be removed. The pin header P-MFG is not stuffed on the PC3-ALLEGRO by default.

P-MFG

P-MFG	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	Entering Manufacturer Mode

[1)] This setting is the factory default

RTC Reset (P-RTC)

The jumper P-RTC may be used to reset certain register bits of the battery backed RTC core within the PCH QM77. This can be necessary under rare conditions (e.g. battery undervoltage), if the CPU fails to enter the BIOS POST after power on. Note that installing of jumper P-RTC will neither set UEFI BIOS Setup to EKF Factory Defaults nor resets the time and date register values of the RTC (Real Time Clock). To reset the RTC core the board must be removed from the system rack. Short-circuit the pins of P-RTC for about 1 sec. Thereafter reinstall the board to the system and switch on the power. It is important to accomplish the RTC reset while the board has no power. The pin header P-RTC is not stuffed on the PC3-ALLEGRO by default.

P-RTC

P-RTC	Function
Jumper Removed [1)]	Normal operation
Jumper Installed	RTC reset performed

[1)] This setting is the factory default.

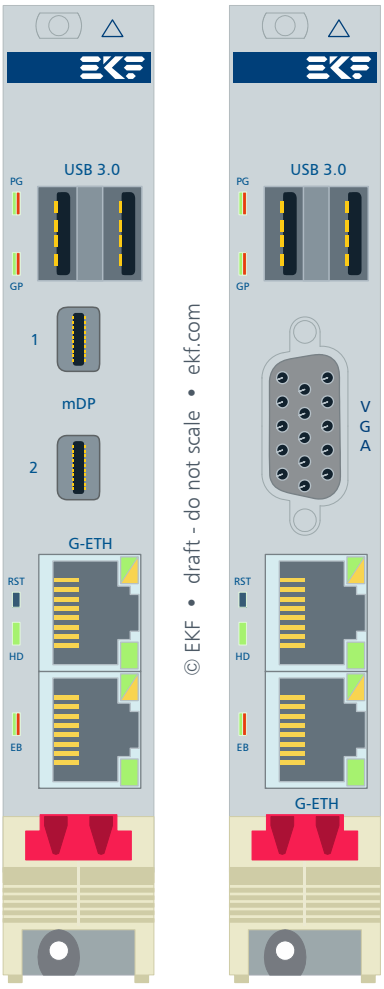
Connectors

Caution

Some of the internal connectors provide operating voltage (3.3V and 5V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are short circuit protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Front Panel Connectors

With respect to the video connector, the PC3-ALLEGRO is available in two flavours, either dual mDP or VGA.

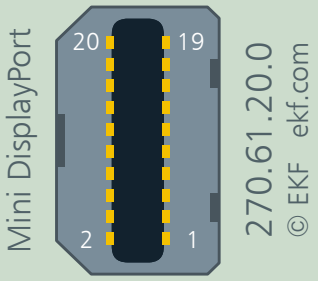


PC3-ALLEGRO
Dual - mDP

PC3-ALLEGRO
VGA

DisplayPort Connectors

The Intel® i7 processors used on PC3-ALLEGRO are equipped with an integrated graphics controller, which supports DisplayPort and SDVO interfaces permitting simultaneous independent operation of up to three displays. Two DP receptacles are available from the PC3-ALLEGRO front panel, as mDP (Mini DisplayPort) connectors, which is a space saving alternate to the standard DP connector and is also specified by the VESA.



Mini DisplayPort J-DP1/2				
	20	PWR [1]	19	GND
	18	AUX_CH(N)	17	LANE2(N)
	16	AUX_CH(P)	15	LANE2(P)
	14	GND	13	GND
	12	LANE3(N)	11	LANE1(N)
	10	LANE3(P)	9	LANE1(P)
	8	GND	7	GND
	6	CONFIG2 (GND)	5	LANE0(N)
	4	CONFIG1	3	LANE0(P)
	2	Hot Plug Detect	1	GND

[1] +3.3V protected by a self resetting PolySwitch fuse 0.75A. This voltage is switched on in S0 state only.

Most DisplayPort monitors come with the standard DP connector, hence requiring a mDP to DP cable assembly for use with the PC3-ALLEGRO. For attachment of either a classic style analog RGB monitor, DVI or HDMI type display to the J-DP receptacles, there are both adapters and also adapter cables available.

Specified by the VESA DisplayPort connector standard is a dedicated power pin 20 (+3.3V 0.5A). Both the GPU (source side) and a DP monitor (sink side) must provide power via this pin. A VESA specified standard DisplayPort cable however must not connect the pins 20 of both cable ends, in order to avoid a back driving conflict. Unfortunately there are cable assemblies available with pin 20 passed through, with unpredictable results on the system behaviour. Before ordering DP cable assemblies, verify the associated wiring diagram.

Sample VESA Compliant Mini DisplayPort Cable Assemblies 2.0m Mini DisplayPort (mDP) to DisplayPort (DP) plug to plug cable assembly, VESA compliant EKF Part. #270.66.2.02.0	
Astron	T2M2M20020-R
Molex	0687850003
Roline	1045636
Wieson	G9858

Screw Locking Option for mDP Connectors

Opposite to the Standard DisplayPort cable connectors, mDP connectors are not provided with a latching device. For rugged applications with need for a connector locking mechanism, EKF offers two methods of fixing.

Option Screw-Lock Plate for mDP Cable Connectors

1. The front panel is provided with a threaded hole for fixing a removable H-shape retainer plate, which is available from EKF as accessory (image above).

2. As an alternate, the customer can use cable assemblies with screw-locked mDP connectors (image below). The front panel has to be modified however for this solution (two threaded holes in addition, please specify when ordering).

Screw-Locked mDP Connector Cable Assembly (Delock)

A third DisplayPort video output is available when combining the PC3-ALLEGRO with the mezzanine side card PCS-BALLET. The standard DP connector is provided with latches, which may be important for some applications.

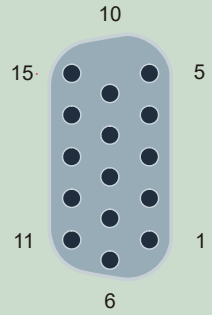
PC3-ALLEGRO w. PCS-BALLET C32-FIO (12HP)

PC3-ALLEGRO w. PCS-BALLET Side Card & 2.5-Inch SSD (8HP)

PC3-ALLEGRO w. PCS-BALLET C32-FIO C20-SATA (12HP)

VGA Video Connector

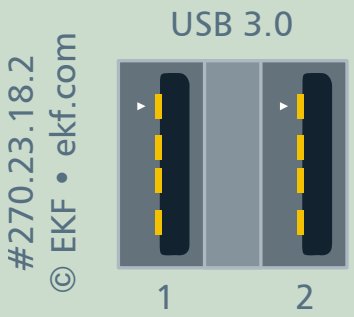
As an option, the PC3-ALLEGRO can be equipped with a legacy VGA connector (High-Density D-Sub 15-position female connector). The connector VGA replaces the two Mini DisplayPort receptacles, and the digital video interface therefore is not available concurrently with this option.

J-VGA (Option)		
	1	RED
	2	GREEN
	3	BLUE
	4	NC
	5	GND
	6	GND
	7	GND
	8	GND
	9	DDC_POW [1)]
	10	GND
	11	NC
	12	VGA_DDC_SDA
	13	HSYNC
	14	VSYNC
	15	VGA_DDC_SCL

[1)] +3.3V protected by a self resetting PolySwitch fuse 0.75A. This voltage is switched on in S0 state only.

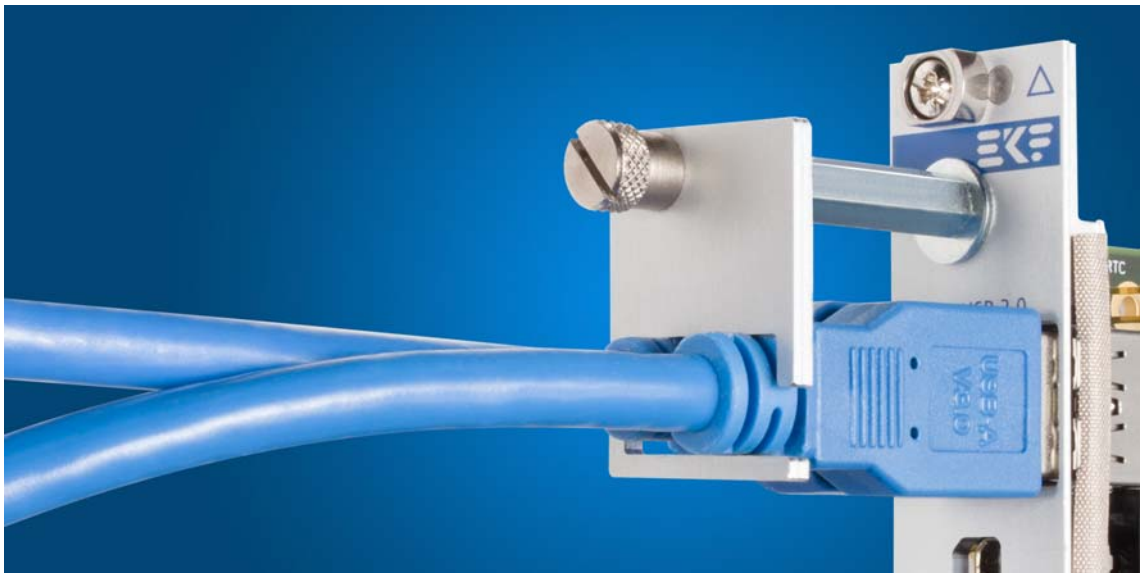
USB Connectors

The Intel® QM77 Platform Controller Hub incorporates a four-port USB 3.0 xHCI host controller. Two ports are directly available on the PC3-ALLEGRO front panel (type A receptacle), for attachment of external USB devices.

USB • Dual USB 3.0 Receptacle USB 3.0 dual type A receptacle, stacked, 18-position		
	1	VBUS +5V, 1.5A max [1]
	2	USB D-
	3	USB D+
	4	GND
	5	SS RX-
	6	SS RX+
	7	GND
	8	SS TX-
	9	SS TX+

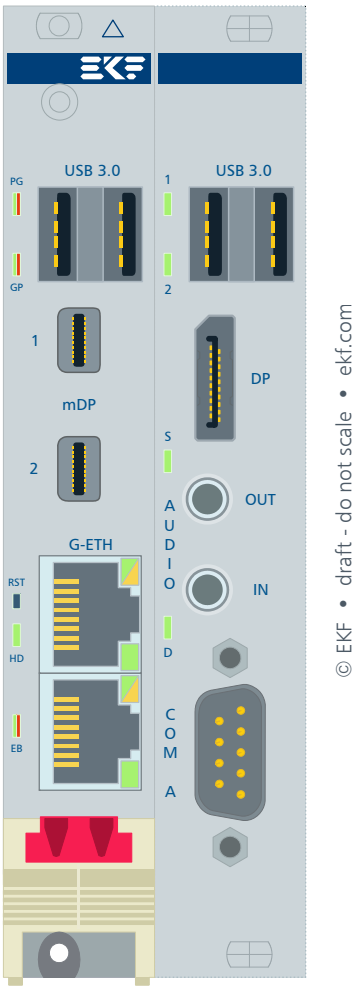
[1] +5V via 1.5A current-limited electronic power switch. Power rail may be switched off by software independently for each port.

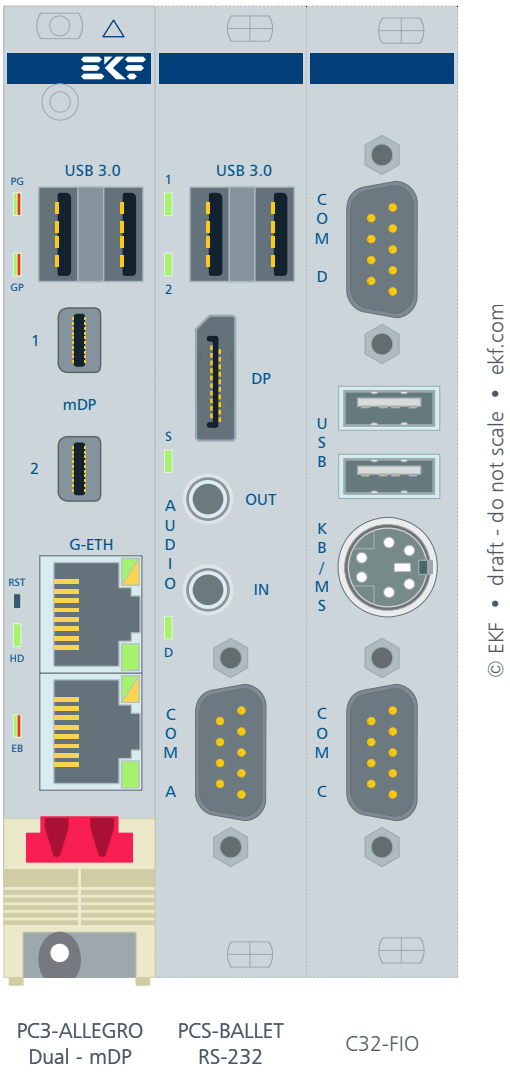
Another two USB 3.0 connectors would be available when the PC3-ALLEGRO is combined with the PCS-BALLET mezzanine side card. EKF offers USB cable connector retainer solutions, for rugged applications (picture below).



Another two USB 3.0 connectors would be available when the PC3-ALLEGRO is combined with the PCS-BALLET mezzanine side card.

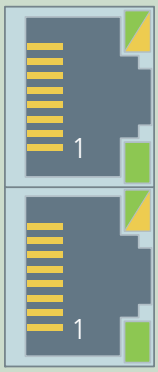
PC3-ALLEGRO w. PCS-BALLET Mezzanine Side Card (8HP)





8HP and 12HP front panel assembly

Ethernet Connectors

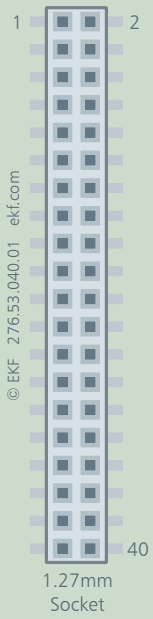
Gigabit Ethernet Ports 1/2 (J-ETH, RJ-45)			
 270.02.08.5	Port 1	1	NC1_MDX0+
		2	NC1_MDX0-
		3	NC1_MDX1+
		4	NC1_MDX2+
		5	NC1_MDX2-
		6	NC1_MDX1-
		7	NC1_MDX3+
		8	NC1_MDX3-
	Port 2	1	NC2_MDX0+
		2	NC2_MDX0-
		3	NC2_MDX1+
		4	NC2_MDX2+
		5	NC2_MDX2-
		6	NC2_MDX1-
		7	NC2_MDX3+
		8	NC2_MDX3-

The lower green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the lower green LED is permanently off, no LINK is established. The upper green/yellow dual-LED signals the link speed 1Gbit/s when lit yellow, 100Mbit/s when lit green, and 10Mbit/s when off.

Mezzanine Connectors

Mezzanine Side Card Connector Suite

Expansion Interface J-EXP

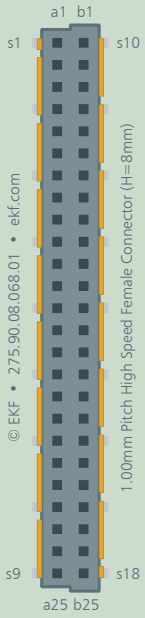
J-EXPT (J-EXPB optinal)				
	GND	1	2	+3.3V [1]
	PCI_CLK (33MHz)	3	4	RST_PLC#
	LPC_AD0	5	6	LPC_AD1
	LPC_AD2	7	8	LPC_AD3
	LPC_FRM#	9	10	LPC_DRQ#
	GND	11	12	+3.3V [1]
	LPC_SERIRQ	13	14	WAKE#
	EXP_SMI#	15	16	SIO_CLK (14.3MHz)
	FWH_ID0	17	18	FWH_INIT#
	KBRST#	19	20	A20GATE
	GND	21	22	+5V [1]
	USB_EXP2-	23	24	USB_EXP1-
	USB_EXP2+	25	26	USB_EXP1+
	USB_EXP_OC#	27	28	DBRESET#
	EXP_SCL [2]	29	30	EXP_SDA [2]
	GND	31	32	+5V [1]
	HDA_SDOUT	33	34	HDA_SDIN0
	HDA_RST#CL_RST# [3]	35	36	HDA_SYNC
	HDA_CLK/CL_CLK [3]	37	38	HDA_SDIN1/CL_DATA [3]
	SPEAKER	39	40	+12V [4]

1) Power rail switched on in state S0 only.
2) Connected to SMBus via buffered switch, isolated after reset.
3) Stuffing option, default is the HDA option.
4) Power rail switch off in state S5.

The expansion interface header footprint is available on both sides of the board, top (J-EXPT) and bottom (J-EXPB). The bottom side connector is stuffed only on customers request.

WARNING: The +3.3V/+5V/+12V power pins are not protected against a short circuit event. The connector J-EXP therefore should be used only for attachment of an approved expansion side card. The maximum current flow across these pins should be limited to 1A per power pin.

High Speed Expansion Connector J-HSE



High Speed Expansion J-HSE			
GND	a1	b1	GND
SATA_HSE1_TXP [5]	a2	b2	SATA_HSE3_TXP [4] [5]
SATA_HSE1_TXN [5]	a3	b3	SATA_HSE3_TXN [4] [5]
GND	a4	b4	GND
SATA_HSE1_RXN [5]	a5	b5	SATA_HSE3_RXN [4] [5]
SATA_HSE1_RXP [5]	a6	b6	SATA_HSE3_RXP [4] [5]
GND	a7	b7	GND
SATA_HSE2_TXP [4] [5]	a8	b8	SATA_HSE4_TXP [5]
SATA_HSE2_TXN [4] [5]	a9	b9	SATA_HSE4_TXN [5]
GND	a10	b10	GND
SATA_HSE2_RXN [4] [5]	a11	b11	SATA_HSE4_RXN [5]
SATA_HSE2_RXP [4] [5]	a12	b12	SATA_HSE4_RXP [5]
GND	a13	b13	GND
USB_HSE1_P	a14	b14	USB_HSE3_P
USB_HSE1_N	a15	b15	USB_HSE3_N
GND	a16	b16	GND
USB_HSE2_P	a17	b17	USB_HSE4_P
USB_HSE2_N	a18	b18	USB_HSE4_N
GND	a19	b19	GND
USB_HSE_OC1#	a20	b20	USB_HSE_OC34#
USB_HSE_OC2#	a21	b21	USB_HSE_OC34#
+3.3VS [1]	a22	b22	+5VS [1]
+3.3VS [1]	a23	b23	+5VS [1]
+3.3VA [2]	a24	b24	+5VA [2]
+12V [3]	a25	b25	+12V [3]

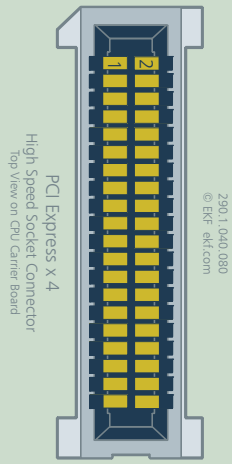
[1] Power rail switched on in state S0 only (Switched).
[2] Power rail on with system stand-by power (Always).
[3] Power rail switch off in state S5.
[4] This SATA channel is capable to perform up to 6Gbps.
[5] All TX/RX designations with respect to the SATA controller.

WARNING: The +3.3V/+5V/+12V power pins are not protected against a short circuit event. The connector J-HSE therefore should be used only for attachment of an approved expansion side card. The maximum current flow through these power pins should be limited to 0.5A per pin.

PC3-ALLEGRO w. C47-MSATA Dual SSD Mezzanine Storage Module

PC3-ALLEGRO w. C48-M2 Dual M.2 SATA SSD Module

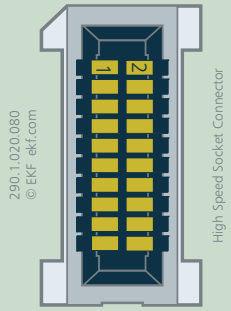
PCI Express® Expansion Header J-PCIE

J-PCIE				
	GND	1	2	GND
	+5V [1]	3	4	+3.3V [1]
	+5V [1]	5	6	+3.3V [1]
	GND	7	8	GND
	PE_CLKP	9	10	PLTRST#
	PE_CLKN	11	12	PE_WAKE#
	GND	13	14	GND
	PE_1TP	15	16	PE_1RP
	PE_1TN	17	18	PE_1RN
	GND	19	20	GND
	GND	21	22	GND
	PE_2TP	23	24	PE_2RP
	PE_2TN	25	26	PE_2RN
	GND	27	28	GND
	PE_3TP	29	30	PE_3RP
	PE_3TN	31	32	PE_3RN
	GND	33	34	GND
	PE_4TP	35	36	PE_4RP
	PE_4TN	37	38	PE_4RN
	GND	39	40	GND

[1] Power rail switched on in state S0 only.

WARNING: The +3.3V/+5V power pins are not protected against a short circuit event. The connector J-PCIE therefore should be used only for attachment of an approved expansion side card. The maximum current flow through these power pins should be limited to 1A per pin.

SDVO/DisplayPort Expansion Header J-SDVO

J-SDVO				
	GND	1	2	GND
	SDVO_RED+/DP_LANE0+	3	4	SDVO_CLK+/DP_LANE3+
	SDVO_RED-/DP_LANE0-	5	6	SDVO_CLK-/DP_LANE3-
	GND	7	8	GND
	SDVO_GREEN+/DP_LANE1+	9	10	SDVO_INT+/DP_AUX+
	SDVO_GREEN-/DP_LANE1-	11	12	SDVO_INT-/DP_AUX-
	GND	13	14	GND
	SDVO_BLUE+/DP_LANE2+	15	16	SDVO_CTR_CLK/DP_HPD
	SDVO_BLUE-/DP_LANE2-	17	18	SDVO_CTR_DATA/DP_CFG1
	GND	19	20	GND

To use J-SDVO as either an SDVO or a further DisplayPort interface, some of the control lines are configurable by a multiplexer. The state of this multiplexer is controlled by PCH QM77 GPIO16 and adjustable by BIOS. Setting GPIO16 to LO configures the connector J-SDVO to work in SDVO mode. In this case pins 10/12 carry the SDVO_INT and pins 16/18 the SDVO_CTR function.
This option was removed with BIOS#126!

With GPIO16 set to HIGH the connector behaves like a DisplayPort interface. The pins 10/12 function as DP_AUX while pin 16 and 18 are connected to DP_HPD and DP_CFG1 respectively.

PC3-ALLEGRO w. PCS-BALLET & Half-Slim SATA SSD (8HP)

PC3-ALLEGRO w. PCS-BALLET & C41-CFAST (8HP)

Typical 8HP Assembly w. PCS-BALLET Side Card & C42-SATA

8HP Assembly w. PCS-BALLET Side Card & C47-MSATA

PC3-ALLEGRO w. PCL-CAPELLA Side Card 8HP Assembly

PC3-ALLEGRO w. PCL-CAPELLA Side Card 8HP Assembly

Pin Headers & Debug

Front Panel Handle Microswitch Header P-FPH

The jumper P-FPH is used for attachment of an external SPDT switch. By default, P-FPH is connected across a short cable harness to a microswitch, which is integrated into the PC3-ALLEGRO front panel handle (ejector lever). The switch performs a power button event (e.g. system shutdown) by short-circuiting the pins 1 and 3 of P-FPH when activated (hold unlock button of front panel handle depressed momentarily).

P-FPH		
# 276.02.003.11 © EKF • ekf.com 		
1	black	Microswitch Pole (Common), Wired to PLD
2	red	Microswitch Throw - F/P Handle Locked Position, NC
3	yellow	Microswitch Throw - F/P Handle Unlocked Position, Wired to GND

PLD Programming Header P-ISP

The PC3-ALLEGRO is provided with a powerful PLD (in-System Programmable Logic Device) which replaces legacy glue logic. The programming header P-ISP is not stuffed (in use for manufacturing only). Its footprint is situated at the bottom side of the board.

P-ISP

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1	+3.3V
2	TDO
3	TDI
4	*NC*
5	*KEY*
6	TMS
7	GND
8	TCK

Processor Debug Header XDP1

The PC3-ALLEGRO may be equipped with a 26-position processor debug header for hard- and software debugging (specified by Intel® as XDP-SFF-26 Pin Platform Connection). The connector is suitable for installation of a flat flex cable (FFC), in order to attach an JTAG debugger (emulator) such as the Arium ECM-XDP3. An adapter (ITP-XDP-SFF-26) is required in addition to convert the 26-pin XDP-SFF-26 Pin connector to the standard 60-pin XDP.

The header XDP1 would be mounted on the PCB bottom side, but is not stuffed by default.

XDP Processor Debug Connector			
269.1.026.902 • FFC Connector  © EKF • ekf.com			
1	OBSFN_A0 (PREQ#)	OBSFN_A1 (PRDY#)	2
3	GND	*OBSDATA_A0*	4
5	*OBSDATA_A1*	GND	6
7	*OBSDATA_A2*	*OBSDATA_A3*	8
9	GND	HOOK0 (CPU_PWRGOOD)	10
11	HOOK1 (XDP_PWRBTN)	HOOK2 (CFG[0])	12
13	HOOK3 (SYS_PWROK)	HOOK4 (BCLKP)	14
15	HOOK5 (BCLKN)	VCCOBS_AB (+1.05V)	16
17	HOOK6 (PLTRST#)	HOOK7 (DBRESET#)	18
19	GND	TDO	20
21	TRST#	TDI	22
23	TMS	*TCK1*	24
25	GND	TCK0 (TCK)	26

Backplane Connectors

CompactPCI J1

J1	A	B	C	D	E
25	5V	*REQ64#* [2]	ENUM# [1]	3.3V	5V
24	AD1	5V	V(I/O)	AD0	*ACK64#* [2]
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	GND/M66EN [7]	C/BE0#
20	AD12	GND	V(I/O)	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR# [1]	GND	3.3V	PAR	C/BE1#
17	3.3V	IPMB SCL [3]	IPMB SDA [3]	GND	PERR# [1]
16	DEVSEL# [1]	GND	V(I/O)	STOP# [1]	LOCK# [1]
15	3.3V	FRAME# [1]	IRDY# [1]	BD_SEL# [6]	TRDY# [1]
14	KEY AREA				
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	GND	AD23	GND	AD22
8	AD26	GND	V(I/O)	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ# [1]	GND	3.3V	CLK	AD31
5	*BRSVP1A5* [4]	*BRSVP1B5* [4]	RST#	GND	GNT#
4	IPMB PWR	GND	V(I/O)	INTP [1]	INTS [1]
3	INTA# [1]	INTB# [1]	INTC# [1]	5V	INTD# [1]
2	*TCK* [4]	5V	*TMS* [4]	*TDO* [4]	*TDI* [4]
1	5V	-12V [5]	*TRST#* [4]	+12V	5V

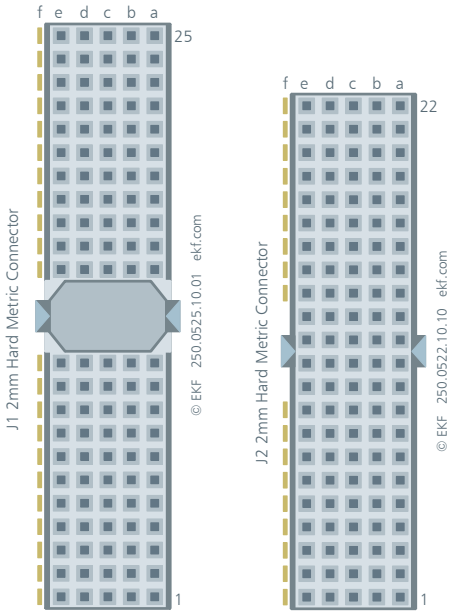
1) This pin is pulled up with 1kΩ to V(I/O).
2) This pin is not used on PC3-ALLEGRO, but pulled up with 1kΩ to V(I/O).
3) This pin is pulled up with 3.0k to J1 pin A4.
4) This pin is not connected.
5) This pin is connected to a decoupling capacitor only and not used on PC3-ALLEGRO.
6) This pin is connected to power sequencing logic and should pulled low for normal operation.
7) This pin can be pulled down on PC3-ALLEGRO to force 33 MHz operation on request. The PC3-ALLEGRO is capable to operate with 66 MHz on the CPCI Bus by default.

CompactPCI J2 (PlusIO)

This connector is a high speed UHM connector, suitable for Gigabit Serial I/O
Refer also to PICMG® 2.30 CompactPCI® PlusIO Specification

J2	A	B	C	D	E
22	*GA4* [2]	*GA3* [2]	*GA2* [2]	*GA1* [2]	*GA0* [2]
21	CLK6	GND	2_ETH_B+ *RSV*	1_ETH_D+ *RSV*	1_ETH_B+ *RSV*
20	CLK5	GND	2_ETH_B- *RSV*	1_ETH_D- *GND*	1_ETH_B- *RSV*
19	GND	GND	2_ETH_A+ *RSV*	1_ETH_C+ *RSV*	1_ETH_A+ *RSV*
18	2_ETH_D+ *BRSVP2A18*	2_ETH_C+ *BRSVP2B18*	2_ETH_A- *BRSVP2C18*	1_ETH_C- *GND*	1_ETH_A- *BRSVP2E18*
17	2_ETH_D- *BRSVP2A17*	2_ETH_C- *GND*	PRST# [1]	REQ6# [1]	GNT6#
16	4_PE_CLK- *BRSVP2A16*	2_PE_CLK+ *BRSVP2B16*	DEG# [1]	GND	reserved [2] *BRSVP2E16*
15	4_PE_CLK+ *BRSVP2A15*	2_PE_CLK- *GND*	FAL# [1] (PSON#) [6]	REQ5# [1]	GNT5#
14	3_PE_CLK- *AD35*	1_PE_CLK+ *AD34*	4_PE_CLKE# *AD33*	SATA_SCL *GND*	reserved [2] *AD32*
13	3_PE_CLK+ *AD38*	1_PE_CLK- *GND*	3_PE_CLKE# *V(I/O)*	SATA_SDO *AD37*	SATA_SL *AD36*
12	4_PE_RX00+ *AD42*	1_PE_CLKE# *AD41*	2_PE_CLKE# *AD40*	SATA_SDI [2] *GND*	4_SATA_RX+ *AD39*
11	4_PE_RX00- *AD45*	4_PE_TX00+ *GND*	4_USB2+ *V(I/O)*	4_SATA_TX+ *AD44*	4_SATA_RX- *AD43*
10	3_PE_RX00+ *AD49*	4_PE_TX00- *AD48*	4_USB2- *AD47*	4_SATA_TX- *GND*	3_SATA_RX+ *AD46*
9	3_PE_RX00- *AD52*	3_PE_TX00+ *GND*	3_USB2+ *V(I/O)*	3_SATA_TX+ *AD51*	3_SATA_RX- *AD50*
8	2_PE_RX00+ *AD56*	3_PE_TX00- *AD55*	3_USB2- *AD54*	3_SATA_TX- *GND*	2_SATA_RX+ *AD53*
7	2_PE_RX00- *AD59*	2_PE_TX00+ *GND*	2_USB2+ *V(I/O)*	2_SATA_TX+ *AD58*	2_SATA_RX- *AD57*
6	1_PE_RX00+ *AD63*	2_PE_TX00- *AD62*	2_USB2- *AD61*	2_SATA_TX- *GND*	1_SATA_RX+ *AD60*
5	1_PE_RX00- *C/BE5#*	1_PE_TX00+ 64EN#	1_USB2+ *V(I/O)*	1_SATA_TX+ *C/BE4#*	1_SATA_RX- *PAR64*
4	V(I/O)	1_PE_TX00- *BRSVP2B4*	1_USB2- *C/BE7#*	1_SATA_TX- *GND*	reserved [2] *C/BE6#*
3	CLK4	GND	GNT3#	REQ4# [1]	GNT4#
2	CLK2	CLK3	SYSEN# [3]	GNT2#	REQ3# [1]
1	CLK1	GND	REQ1# [1]	GNT1#	REQ2# [1]

1) This pin is pulled up with 1kΩ to V(I/O). Alternate pull up resistor values (e.g. 2.7kΩ for V(I/O)=+3.3V) are available on request.
2) This pin is not connected.
3) This pin is pulled up with 10kΩ to +3.3V.
4) *Pin positions printed italic: 64-bit system slot signals (for reference only).*
5) Pin positions printed blue: PlusIO options.
6) As an exclusive stuffing option J2-C15 can be utilised as PSON# output.



J2 UHM (Upper)
J1 (Lower)

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